晶采光電科技股份有限公司
AMPIRE CO., LTD.

Specifications for LCD module

Customer	
Customer part no.	
Ampire part no.	**AM-1024600D8TZQW-00H-A**
Approved by	
Date	

☐ **Preliminary Specification**
■ **Formal Specification**

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Approved by	Checked by	Organized by
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This Specification is subject to change without notice.

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2025/05/26	-	New release	Simon

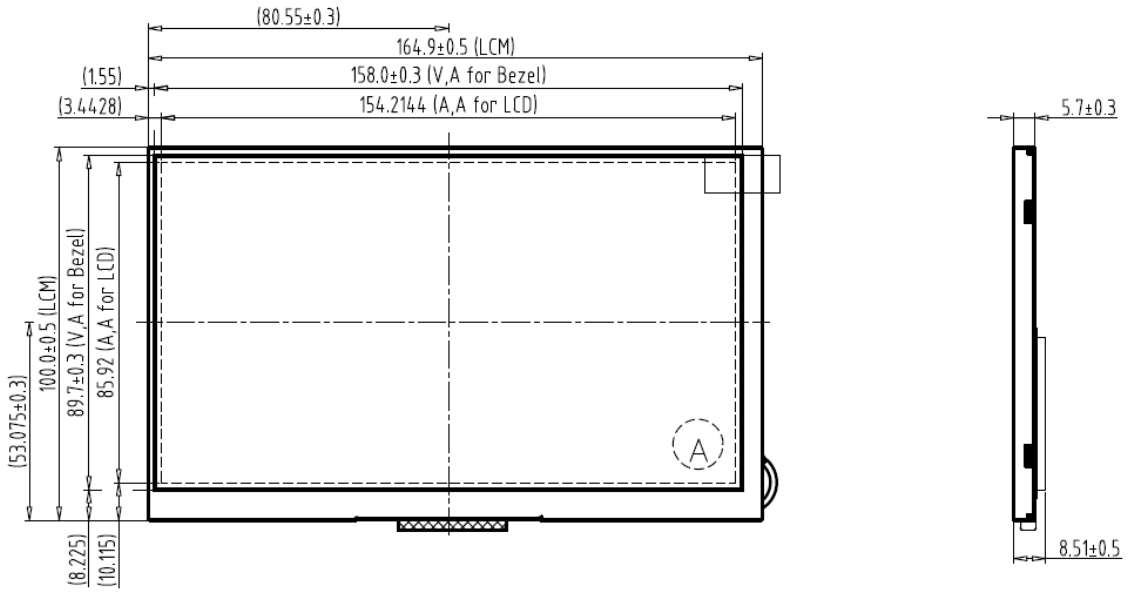
1. Features

It's a 7 inches Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 7" TFT-LCD panel, LED backlight.

(1) Construction: 7" a-Si TFT active matrix, White LED Backlight.
(2) Resolution (pixel): 1024 RGB (H) x 600 (V)
(3) Number of the Colors : 16.7M colors (R , G , B 8 bit digital each), 8-bit resolution 256 gray-scale with dithering(6-bits DAC +2 bits FRC or HFRC)
(4) LCD type : Normally Black
(5) Interface: MIPI
(6) New FPC & LED Driver IC: TPS61185RGER(TI)

2. Physical Specification

Item	Specifications	unit
LCD size	7 inch (Diagonal)	
Resolution	1024 x (RGB) x 600	dot
Pixel pitch	0.1506(W) x 0.1432(H)	mm
Color arrangement	RGB-stripe	



3. Absolute Max. Ratings

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power Voltage	VDD	--	4	V	
LED Driver Power Voltage	VLED	-0.3	19	V	
Operation Temperature	TOP	**-20**	**70**	℃	
Storage Temperature	TST	**-30**	**80**	℃	

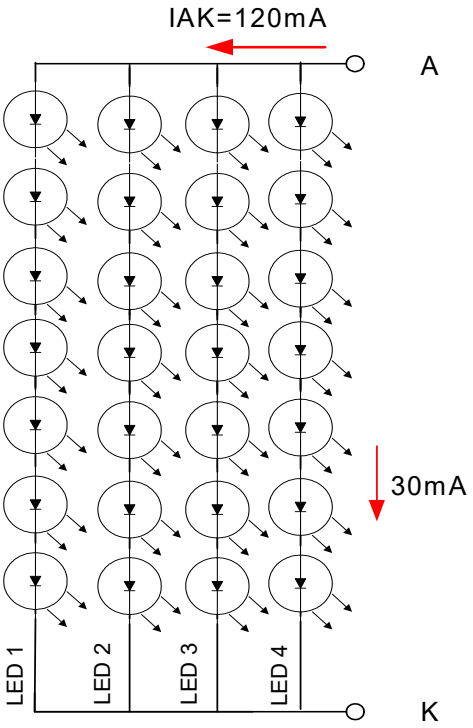
Note(1) The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

4. Backlight Driving Conditions

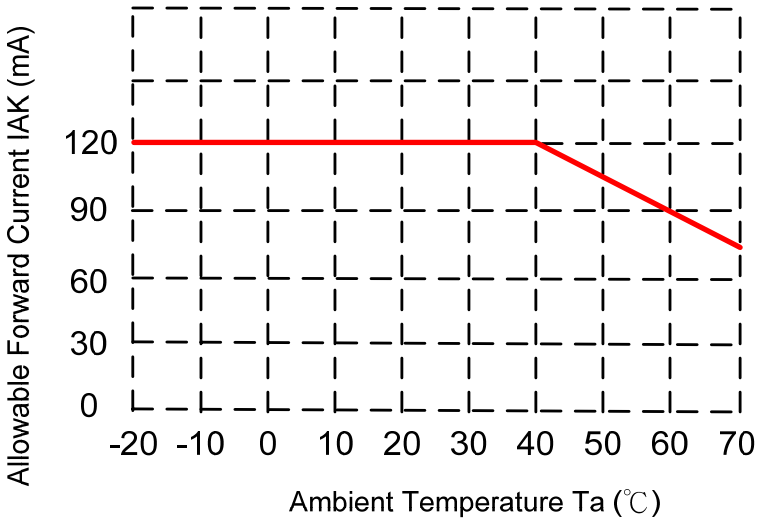
Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Driver Power Voltage	VLED	--	12	19	V	
LED Driver Power Current	ILED(VLED=12V)	--	289	--	mA	Ta=25℃
PWM Dimming DC active level	VDIMH	1.5	--	6	V	
	VDIML	--	--	0.6	V	
PWM Dimming Freq.	FDIM	0.2		20	kHz	
BLEN Pin High Voltage	VBLENH	1.4		--	V	
BLEN Pin Low Voltage	VBLENL	--		0.8	V	
LED voltage	VAK	--	23.1	--	V	Note(1)
LED current	IAK	--	120	--	mA	Note(1)
LED life time	--	--	30	--	kHrs	Note(2)

Note(1) The LED Supply Voltage is defined by the number of LED at Ta=25℃ and IAK=120 mA.

Note(2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IAK=120mA. The LED lifetime could be decreased if operating IAK is larger than 120mA.



Note(3) When LCM is operated over 40℃ ambient temperature, the IAK should be follow :



5. Optical Specifications

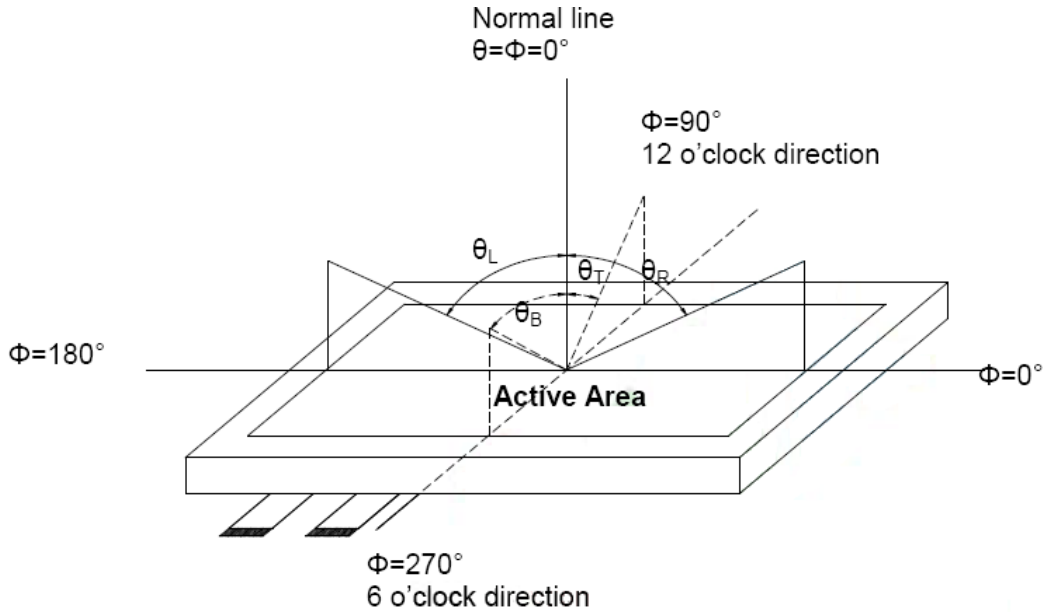
Item	Symbol	Condition	Values			Unit	Note
			Min.	Typ.	Max.		
Viewing angle (CR≧10)	θL	Φ = 180° (9 o'clock)	80	85	--	degree	Note(1)
	θR	Φ = 0° (3 o'clock)	80	85	--		
	θT	Φ = 90° (12 o'clock)	80	85	--		
	θB	Φ = 270° (6 o'clock)	80	85	--		
Response time	TON	Normal θ=Φ=0°	--	13	20	msec	Note(3)
	TOFF		--	15	25	msec	
Contrast ratio	CR		600	800	--	--	Note(4)
Color chromaticity	WX		Typ. -0.05	0.31	Typ. +0.05	--	Note(5) Note(6)
	WY			0.36		--	
	RX			0.61			
	RY			0.34			
	GX			0.36			
	GY			0.57			
	BX			0.10			
	BY			0.08			
Luminance (central point)	L		**400**	**500**	--	cd/m^2	Note(6)
Luminance uniformity	YU		70	75	--	%	Note(6)

Test Conditions:

VDD = 3.3V, IAK = 120 mA (Backlight current), the ambient temperature is 25℃.

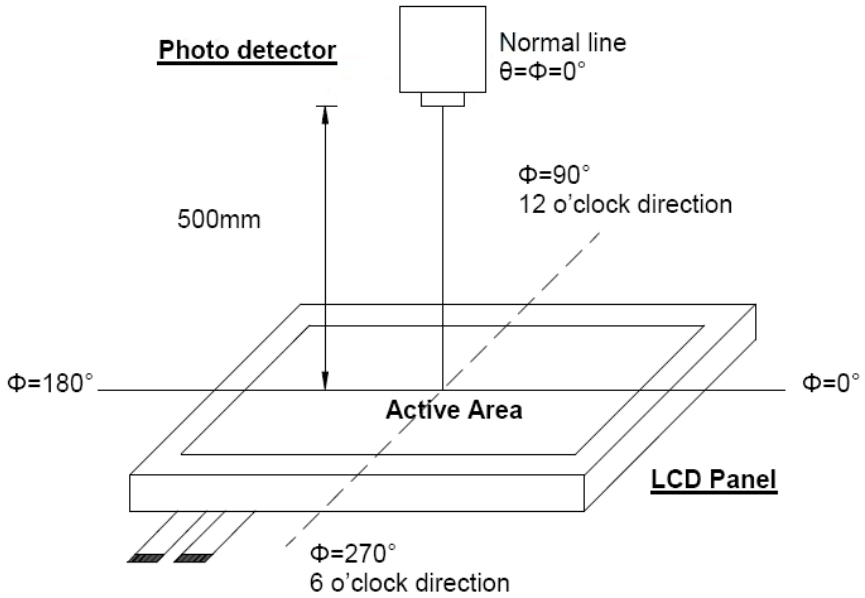
The test systems refer to Note (2).

Note(1) Definition of viewing angle range



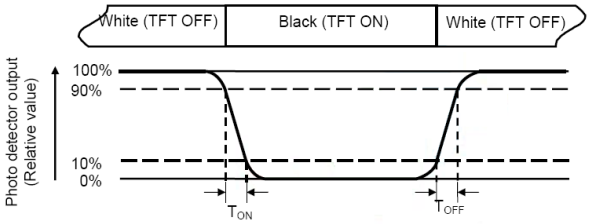
Note(2) Definition of optical measurement system

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° / Height: 500mm.)



Note(3) Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note(4) Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Note(5) Definition of color chromaticity (CIE1931)

Color coordinated measured at center point of LCD.

All input terminals LCD panel must be ground when measuring the center area of the panel.

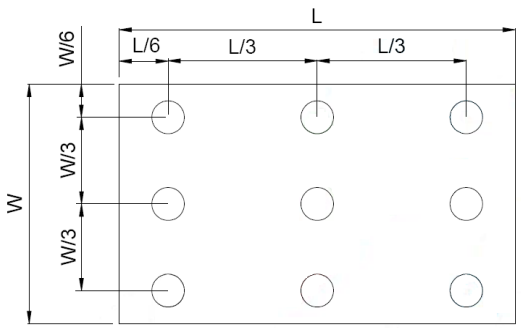
Note(6) Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to bellow figure).

Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (Yu)} = \frac{\text{Bmin}}{\text{Bmax}}$$

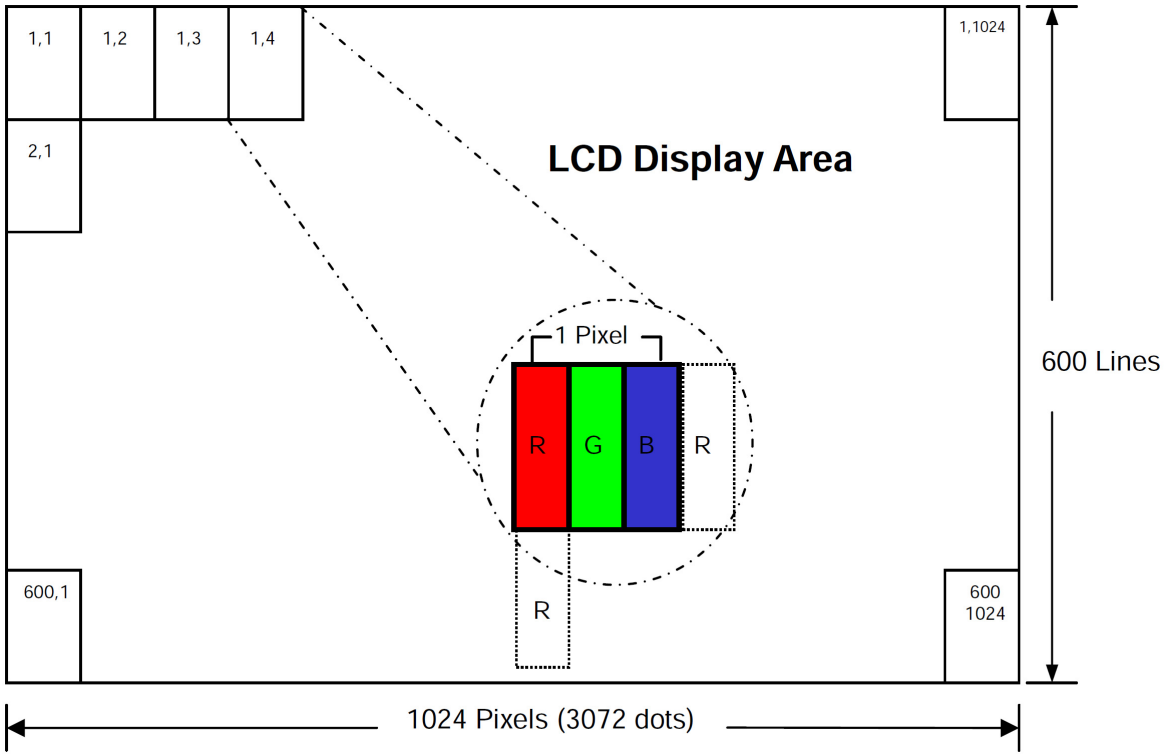
L ----- Active area length W ----- Active area width



Bmax : The measured maximum luminance of all measurement position.

Bmin : The measured minimum luminance of all measurement position.

6. Pixel format



7. Interface

Pin No.	Symbol	Function
1	VDD	Power Supply Voltage
2	VDD	Power Supply Voltage
3	VDD	Power Supply Voltage
4	LED_EN	LED Driver Enable
5	LED_PWM	LED Driver PWM
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	GND	Ground
10	D2P	MIPI data pair 2 positive signal
11	D2N	MIPI data pair 2 negative signal
12	GND	Ground
13	D1P	MIPI data pair 1 positive signal
14	D1N	MIPI data pair 1 negative signal
15	GND	Ground
16	CLKP	MIPI Clock positive signal
17	CLKN	MIPI Clock negative signal
18	GND	Ground
19	D0P	MIPI data pair 0 positive signal
20	D0N	MIPI data pair 0 negative signal
21	GND	Ground
22	D3P	MIPI data pair 3 positive signal
23	D3N	MIPI data pair 3 negative signal
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	NC	No Connection
29	RST	Reset
30	NC	No Connection
31	VLED	LED Driver Power Supply
32	VLED	LED Driver Power Supply
33	VLED	LED Driver Power Supply
34	VLED	LED Driver Power Supply

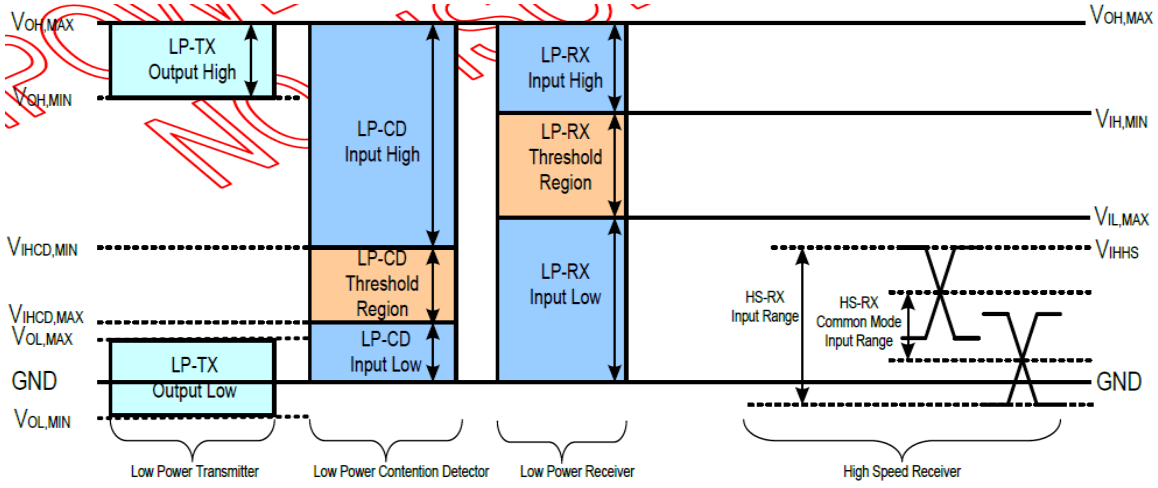
8. Electrical Characteristics

8.1 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Digital Power Supply Voltage	VDD	--	3.3	--	V	
Digital Power Supply Current	IDD		**150**		mA	

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CDRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}		100		ohm
HS transmit differential voltage(VOD=VDP-VDN)	$\|V_{OD}\|$	140	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50		1350	mV
Ground shift	V_{GNDSH}	-50	-	50	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Input hysteresis	V_{HYST}	25	-	-	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	Z_{OLP}	80	100	125	ohm
Logic 0 contention threshold	$V_{ILCD,MAX}$	-	-	200	mV
Logic 0 contention threshold	$V_{IHCD,MIN}$	450	-	-	mV

(VDD_IF=1.8V,AVDD=8 to 13.5V,GND=AGND=GND_IF=0V,TA=-20℃ to 85℃)



8.2 AC Characteristics

8.2.1 Input Timing Table (4Lane)

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2	67.2	Mhz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	Tvd		600		H
VSYNC period time	Tv	610	635	800	H
VSYNC blanking	Tvb+Tvfp	10	35	200	H

HV mode (Horizontal input timing)

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	63	Mhz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			70		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

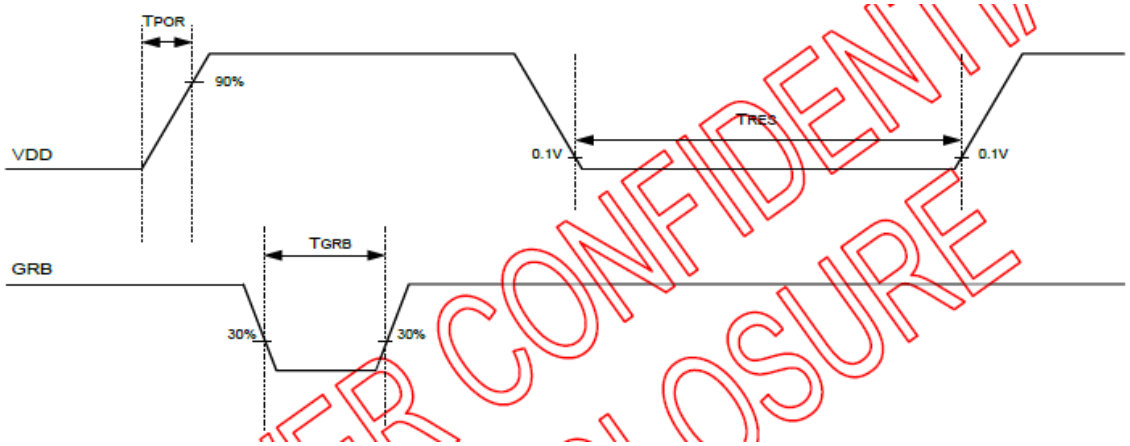
HV mode (Vertical input timing)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	10	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	127	H

8.2.2 VDD/GRB AC characteristics

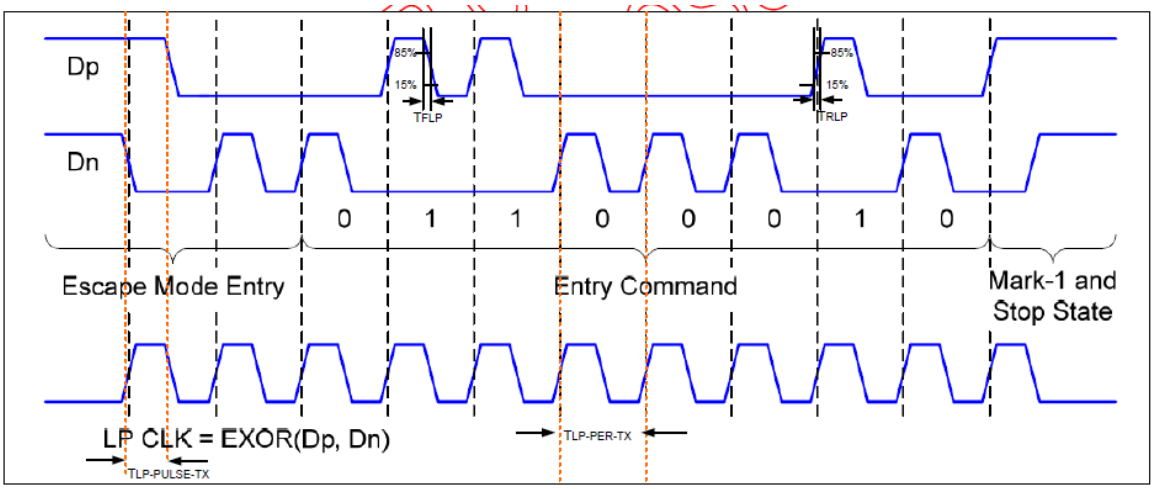
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD power slew rate	T_{POR}	-	-	20	ms	From 0 to 90% VDD
GRB active pulse width	T_{GRB}	1	-	-	ms	VDD=VDD_IF= 1.8V
VDD resettle time	T_{RES}	1	-	-	s	

(VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V,TA=-20 to +85℃)



8.2.3 LP Transmitter AC Specification

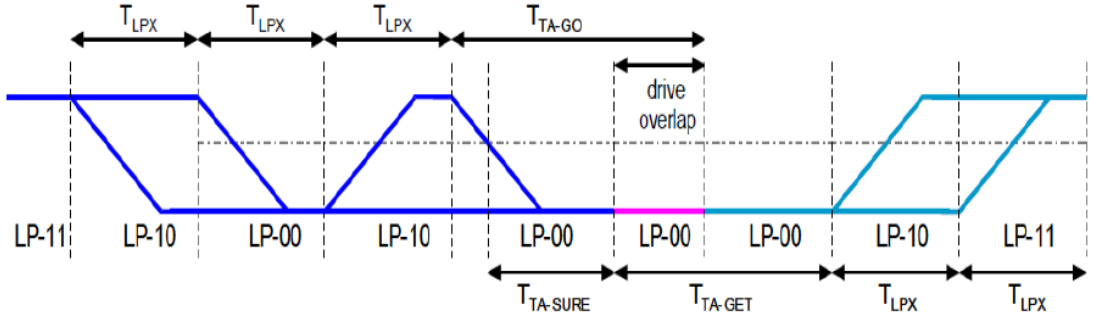
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	-
	All other pulses		20	-	-	ns	-
Period of the LP EXOR clock		$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @C_{LOAD} =0pF		δ V/δ t_{SR}	30	-	500	mV/ns	-
Slew Rate @C_{LOAD} =5pF			30	-	200	mV/ns	-
Slew Rate @C_{LOAD} =20pF			30	-	150	mV/ns	-
Slew Rate @C_{LOAD} =70pF			30	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-



8.2.4 Turnaround Procedure

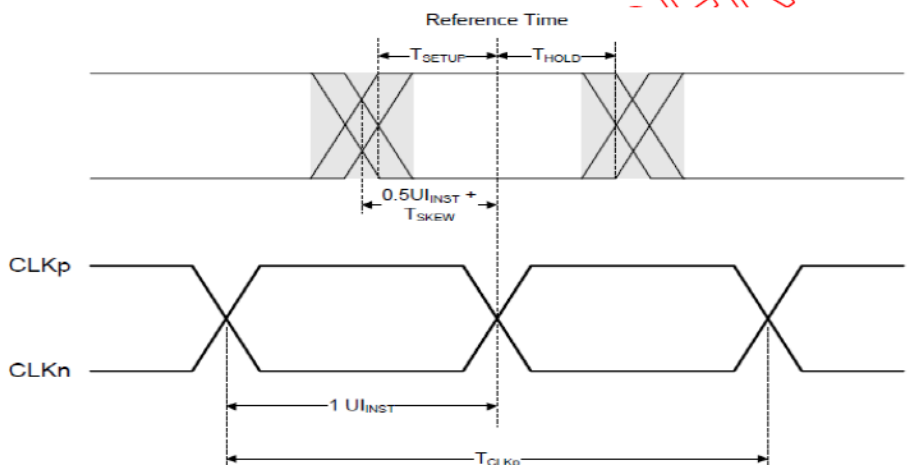
Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period: Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period: Slave side	T_{LPX}	50	55.56	58.34	ns
Ratio of T_{LPX}(Master)/ T_{LPX} (Slave) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	-	2T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	5T_{LPX}	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	4T_{LPX}	-	ns



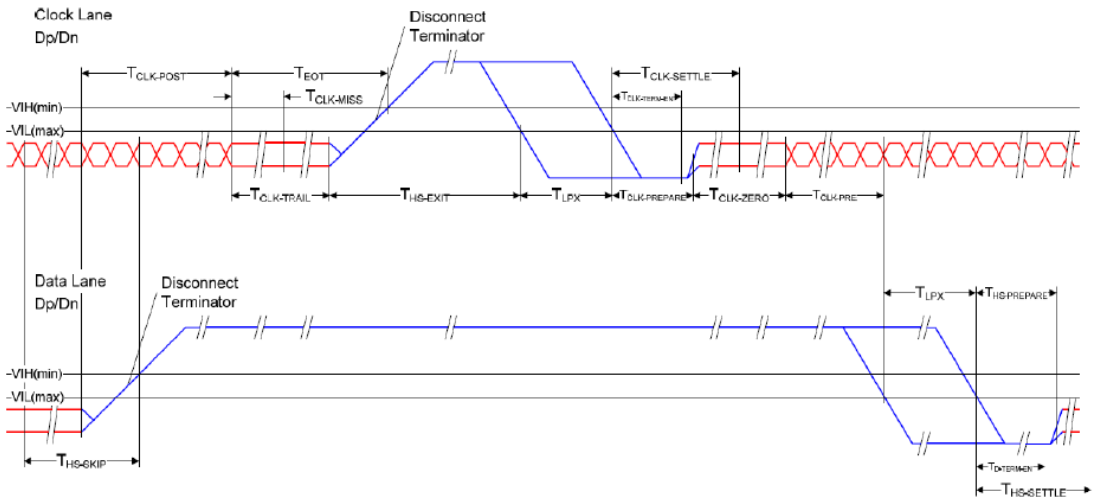
8.2.5 High speed transmission

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter)	$T_{SKEW(TX)}$	-0.15	-	0.15	UI_{INST}
Data to Clock Setup time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to Clock Hold time(measured at receiver)	$T_{HOLD(RX)}$	0.15	-	-	UI_{INST}
20%~80% rise time and fall time	T_R, T_F	150	-	-	ps
		-	-	0.3	UI_{INST}

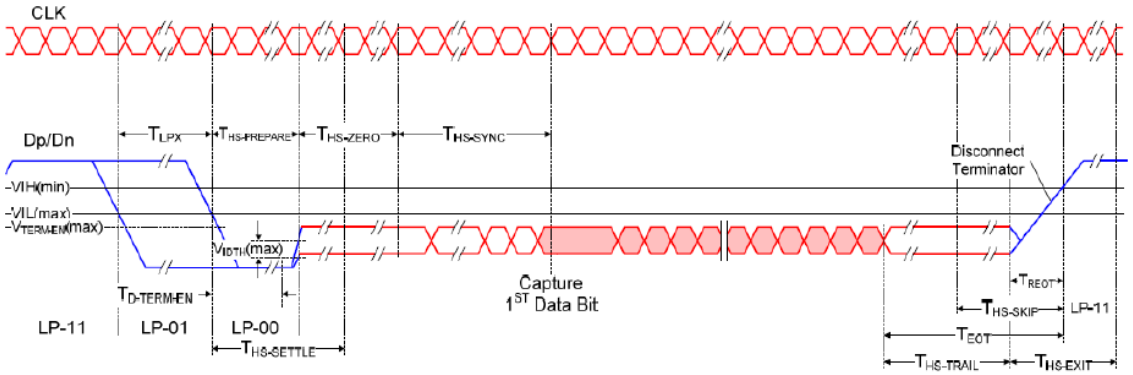


8.2.6 High Speed Clock Transmission

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns



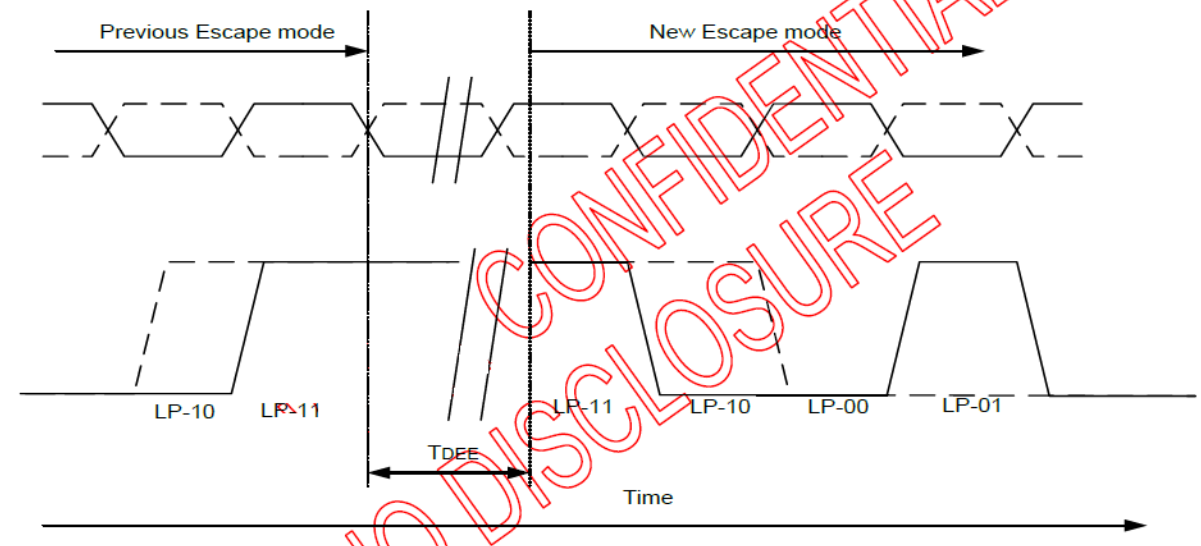
8.2.7 High Speed Data Transmission in Bursts



8.2.8 LP11 timing request between data transformation

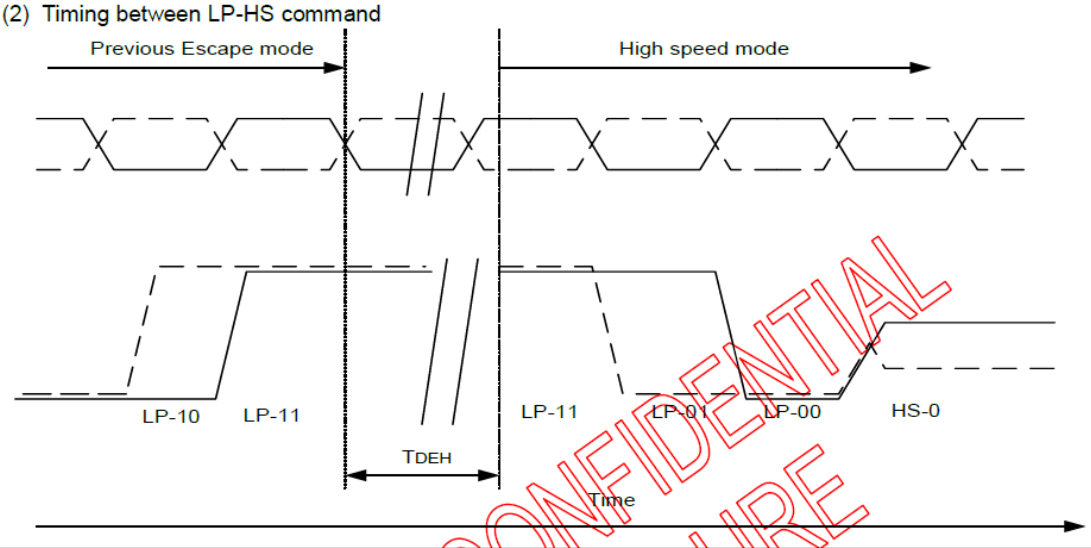
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP—LP, LP—HS, HS—LP, HS—HS, BTA— BTA, LP— BTA, BTA— LP, HS— BTA, and BTA— HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP-LP command



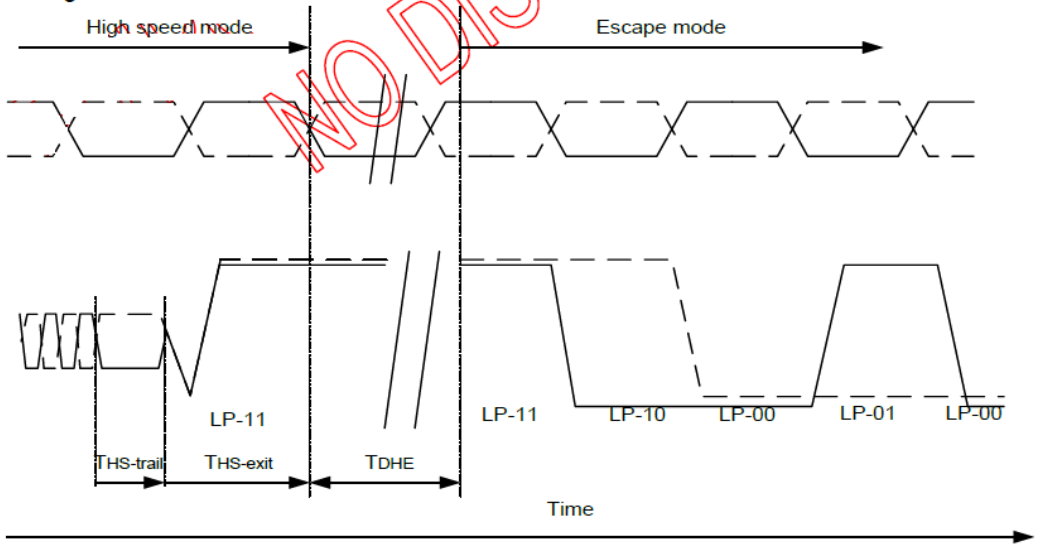
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new Escape Mode Entry	TDEE	150	-	-	ns

(2) Timing between LP-HS command



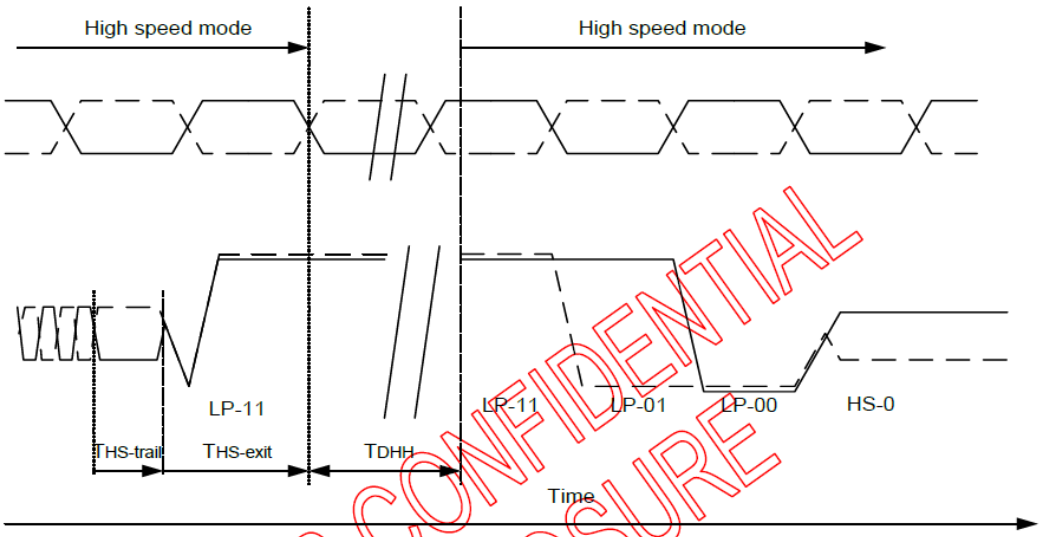
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDEH	Max(150,32UI)	-	-	ns

(3) Timing between HS-LP command



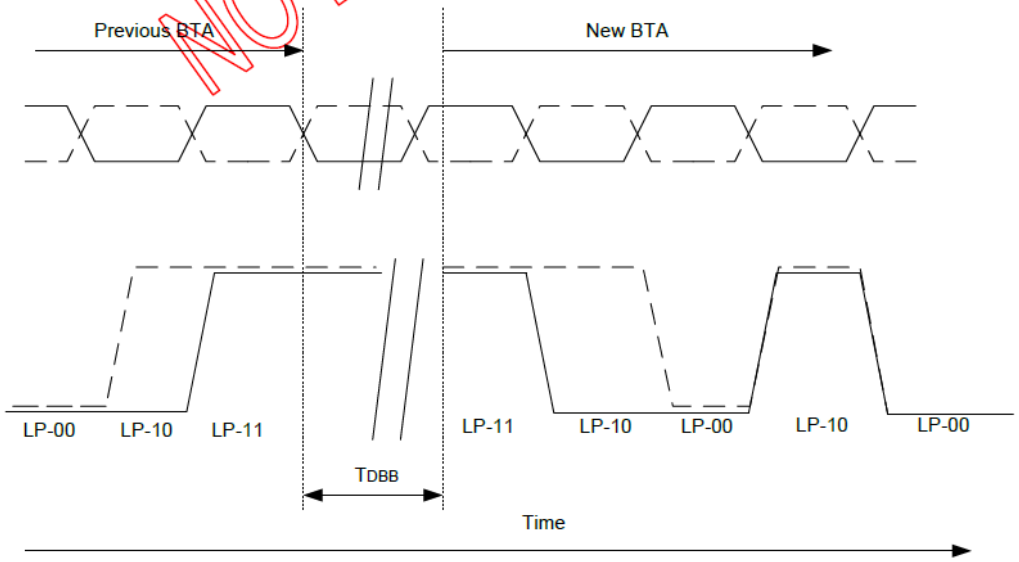
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDHE	Max(150,32UI)	-	-	ns

(4) Timing between HS-HS command



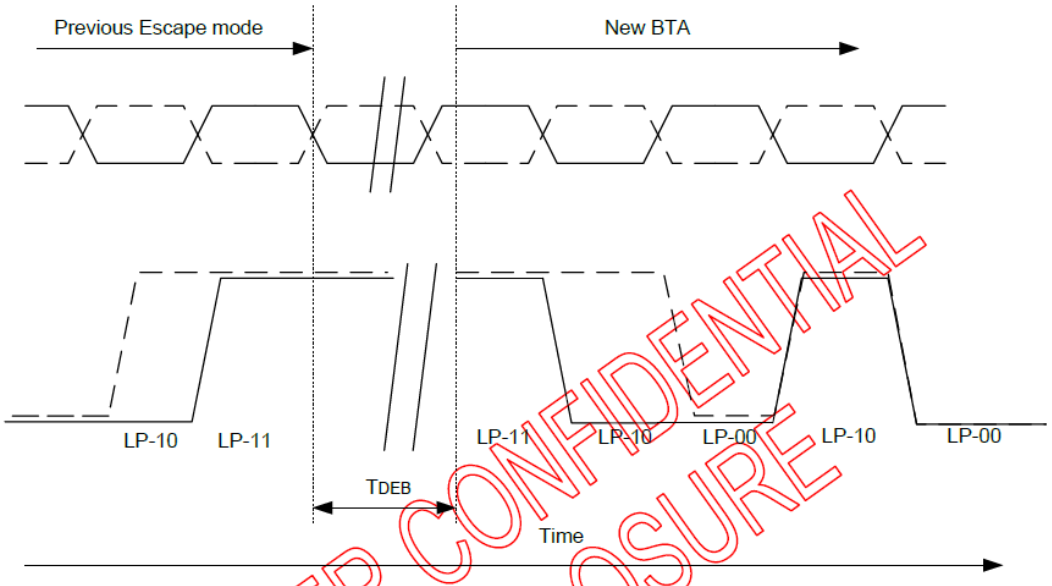
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDHH	Max(150,32UI)	-	-	ns

(5) Timing between BTA-BTA command



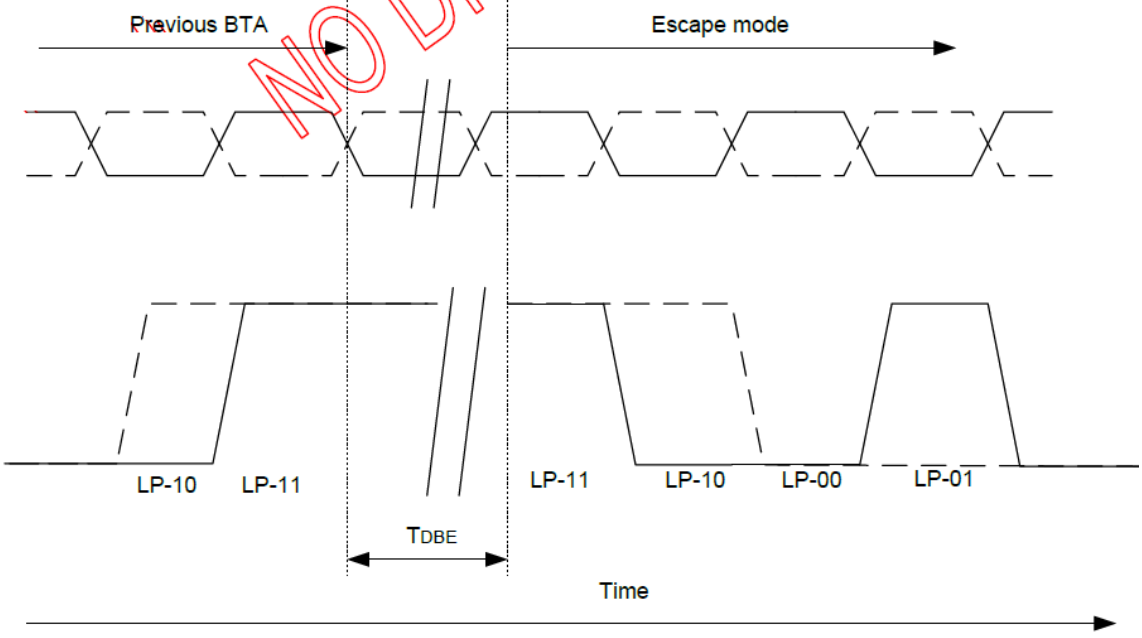
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	TDBB	150	-	-	ns

(6) Timing between LP-BTA command



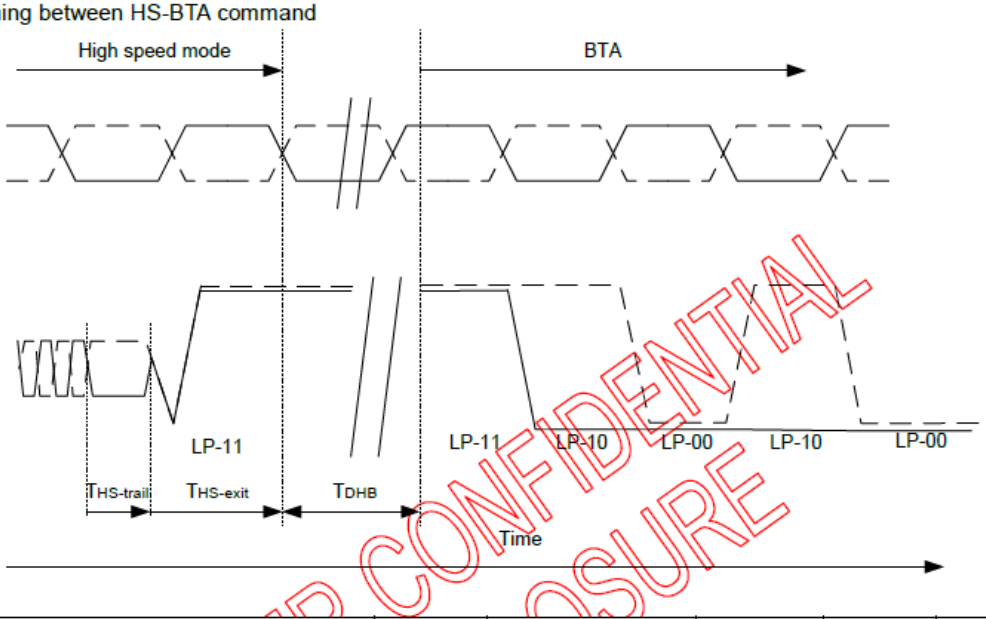
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	T_{DEB}	150	-	-	ns

(7) Timing between BTA-LP command



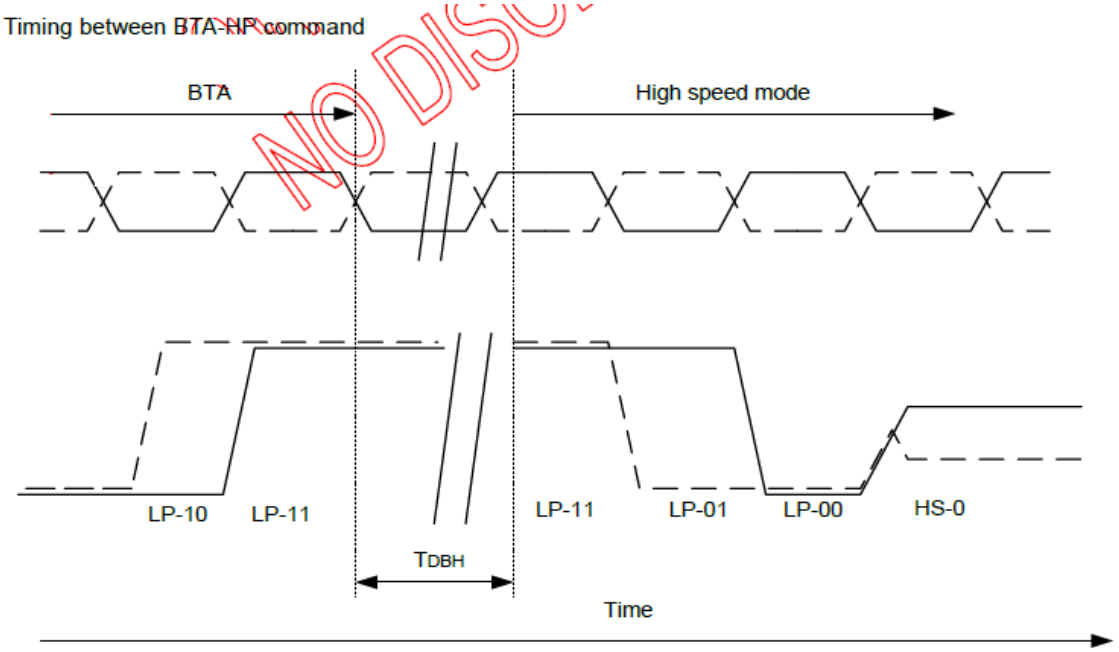
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	T_{DBE}	150	-	-	ns

(8) Timing between HS-BTA command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the BTA	TDHB	Max(150,32UI)	-	-	ns

(9) Timing between BTA-HP command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDBH	Max(150,32UI)	-	-	ns

8.2.9 Display Serial Interface (DSI)

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

8.2.10 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

Non-Burst Mode with Sync Pulses — enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

Non-Burst Mode with Sync Events — similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

Burst mode — RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

During the BLLP the DSI Link may do any of the following:

Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.

Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.

Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.

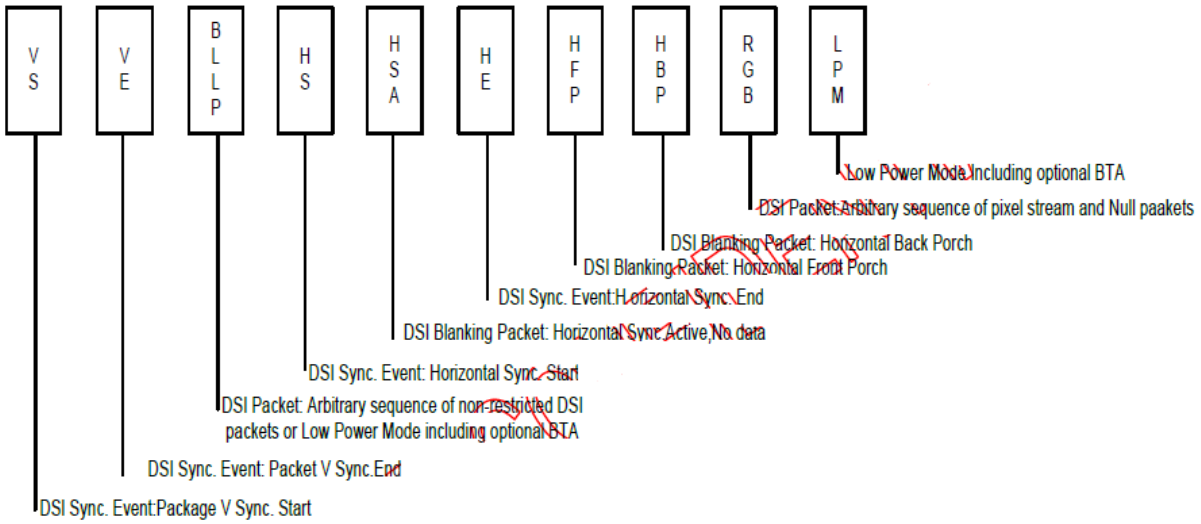
If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.

Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



8.2.11 DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding

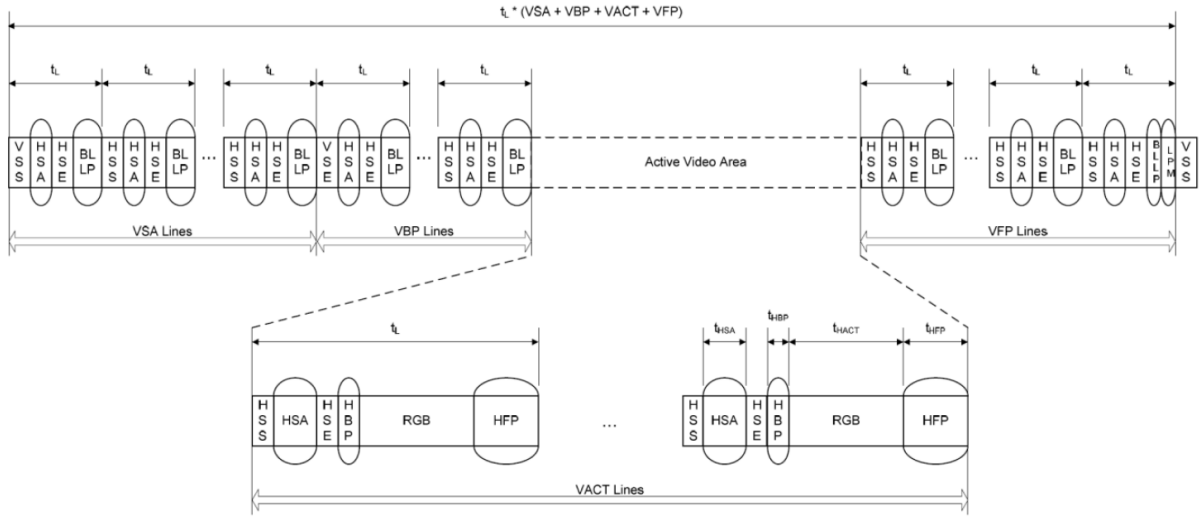
Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

8.2.12 Clock Requirements

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

8.2.13 Non-Burst Mode with Sync Pulses

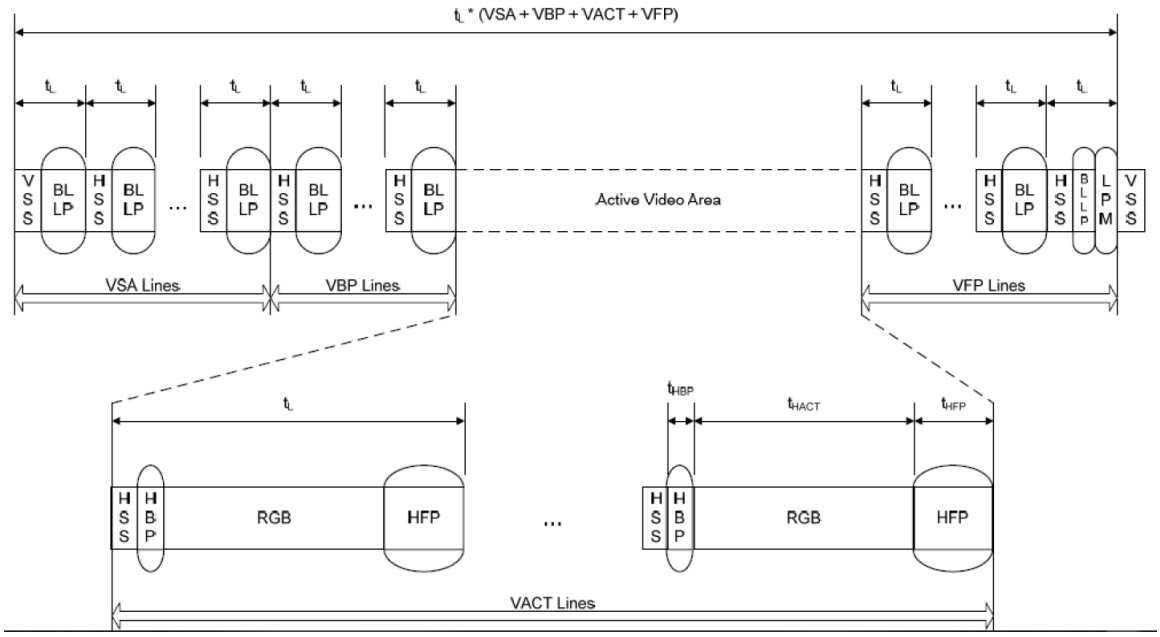
With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.



Normally, periods shown as I (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.2.14 Non-Burst Mode with Sync Events

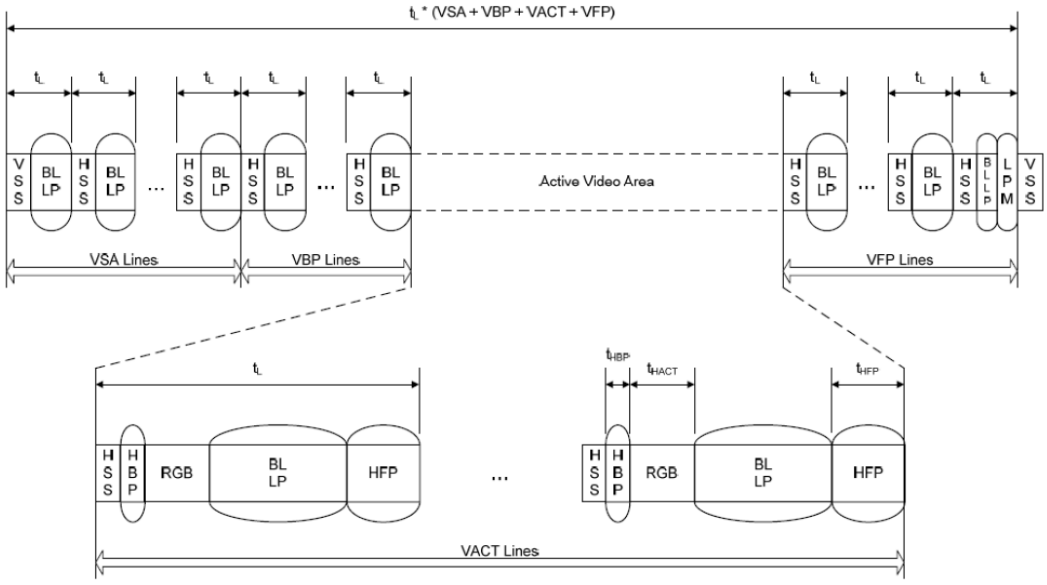
This mode is a simplification of the format described in section “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.



As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.2.15 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

9. Command Description

9.1 MIPI Control Register

Following table list all the MIPI control registers and bit name definition for IC. Refer to the next section for detail register function description, please.

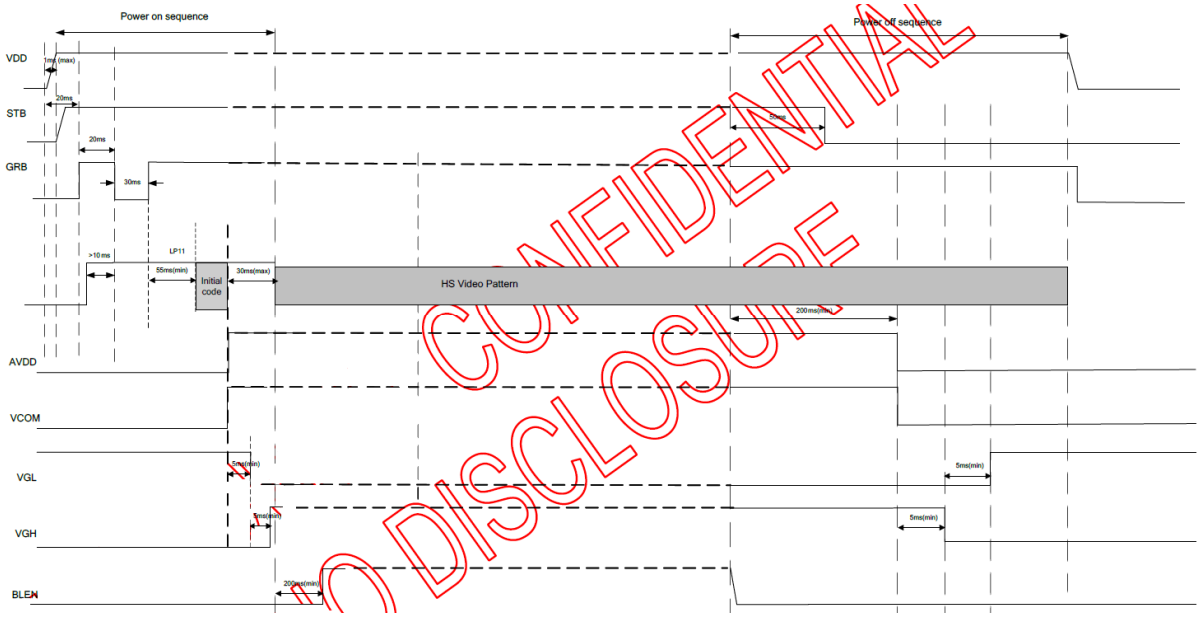
Setting of all the MIPI registers will take effect at the coming valid Vsync signal except GRB bit.

All the MIPI control registers and bit name definition:

	Register address								MSB							LSB	default (hex)
No.	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	DI	DO	–
R00h	0	0	0	0	0	0	0	0	0	NOP								–
R01h	0	0	0	0	0	0	0	1	0	GRB								–
R05h	0	0	0	0	0	0	0	1	0	RDNUMED(TBD)								–
R0Ah	0	0	0	0	1	0	1	0	1	GET_POWER_Mode								–
R0Dh	0	0	0	0	1	1	0	1	1	GET_DISPLAY_Mode								–
R0Eh	0	0	0	0	1	1	1	0	1	GET_SIGNAL_Mode(TBD)								–
R0Fh	0	0	0	0	1	1	1	1	1	RDDSDR(TBD)								–
R10h	0	0	0	1	0	0	0	0	0	ENTER_SLEEP_MODE								–
R11h	0	0	0	1	0	0	0	1	0	EXIT_SLEEP_MODE								–
R20h	0	0	1	0	0	0	0	0	0	EXIT_INVERT_MODE								–
R21h	0	0	1	0	0	0	0	1	0	ENTER_INVERT_MODE								–
R36h	0	0	1	1	0	1	1	0	1/0	0	0	0	0	0	0	UPDN(0)	SHLR(1)	01
R80h	1	0	0	0	0	0	0	0	1/0	G2R[3:0] (1000)				G1R[3:0] (1000)				88
R81h	1	0	0	0	0	0	0	1	1/0	G4R[3:0] (1000)				G3R[3:0] (1000)				88
R82h	1	0	0	0	0	0	1	0	1/0	G6R[3:0] (1000)				G5R[3:0] (1000)				88
R83h	1	0	0	0	0	0	1	1	1/0	G8R[3:0] (1000)				G7R[3:0] (1000)				88
R84h	1	0	0	0	0	1	0	0	1/0	G10R[3:0] (1000)				G9R[3:0] (1000)				88
R85h	1	0	0	0	0	1	0	1	1/0	G12R[3:0] (1000)				G11R[3:0] (1000)				88
R86h	1	0	0	0	0	1	1	0	1/0	G14R[3:0] (1000)				G13R[3:0] (1000)				88
RB0h	1	0	1	1	0	0	0	0	1/0	PWR_EN(0)	–	–	–	–	–	–	–	00
RB1h	1	0	1	1	0	0	0	1	1/0			HFRC(0)	DITHER(0)	BIST(0)	RES[1:0] (00)		–	00
RB2h	1	0	1	1	0	0	1	0	1/0	–	NBW(0)	En_3lane(0)	En_2lane(0)	–	–	–	–	00
RB3h	1	0	1	1	0	0	1	1	1/0	–	–	–	–	–	FRAME(0)	SEL[1:0]		00

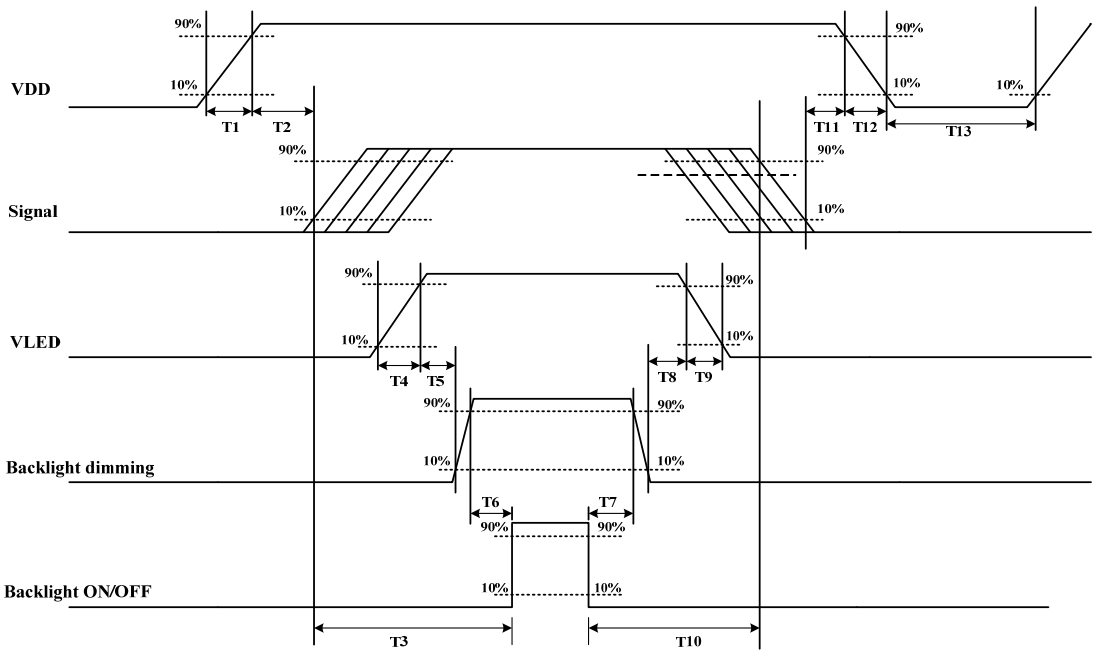
10. Power ON/OFF sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply. VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.



Note: CLK and Data Lanes should keep in LP11 (stop state) before GRB.

VDD power and LED on/off sequence are as follows. Interface signals are also shown in the chart. Signal shall be Hi-Z state or low level when VDD is off.



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	0	40	50	[ms]
T3	200	-	-	[ms]
T4	0.5	-	10	[ms]
T5	10	-	-	[ms]
T6	10	-	-	[ms]
T7	0	-	-	[ms]
T8	10	-	-	[ms]
T9	-	-	10	[ms]
T10	110	-	-	[ms]
T11	0.5	16	50	[ms]
T12	-	-	100	[ms]
T13	1000	-	-	[ms]

11. Reliability Test Conditions

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Storage at High Temperature and Humidity	60°C, 90% RH , 240 hrs	1,2

Note(1) Condensation of water is not permitted on the module.

Note(2) The module should be inspired after 1 hour storage in normal conditions (15~35℃, 45~65%RH).

Note(3) The module shouldn't be tested over one condition, and all the tests are independent.

Note(4) All reliability tests should be done without the protective film.

Definitions of life end point:

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of initial value.

12. General Precautions

12.1 Safety

(1) Liquid crystal is poisonous. Do not put it your month. If the liquid crystal touches you skin or clothes, you need to wash it off immediately with the soap and water.

12.2 Handling

(1) The LCD panel is plate glass. Do not subject the panel to mechanical shock or excessive force on its surface.

(2) The polarizer which attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.

(3) To avoid contamination on the display surface, do not touch the module surface with bare hands.

(4) Keep a space so that the LCD panels do not touch other components.

(5) Put on cover board such as acrylic board, which covers on the surface of LCD panel to protect panel from damages.

(6) Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.

(7) Do not leave module in direct sunlight to avoid malfunction of the ICs.

12.3 Mechanism

(1) Please mount LCD module by using mounting holes arranged in four corners tightly.

12.4 Static Electricity

(1) Be sure to ground module before you turn on power or operation module.

(2) Do not apply voltage which exceeds the absolute maximum rating value.

12.5 Storage

(1) Store the module in a dark room where it must keep at +25±10℃ and 65%RH or less.

(2) Do not store the module in surroundings which are containing organic solvent or corrosive gas.

(3) Store the module in an anti-electrostatic container or bag.

12.6 Cleaning

(1) Do not wipe the polarizer with dry cloth. It might cause scratch.

(2) Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

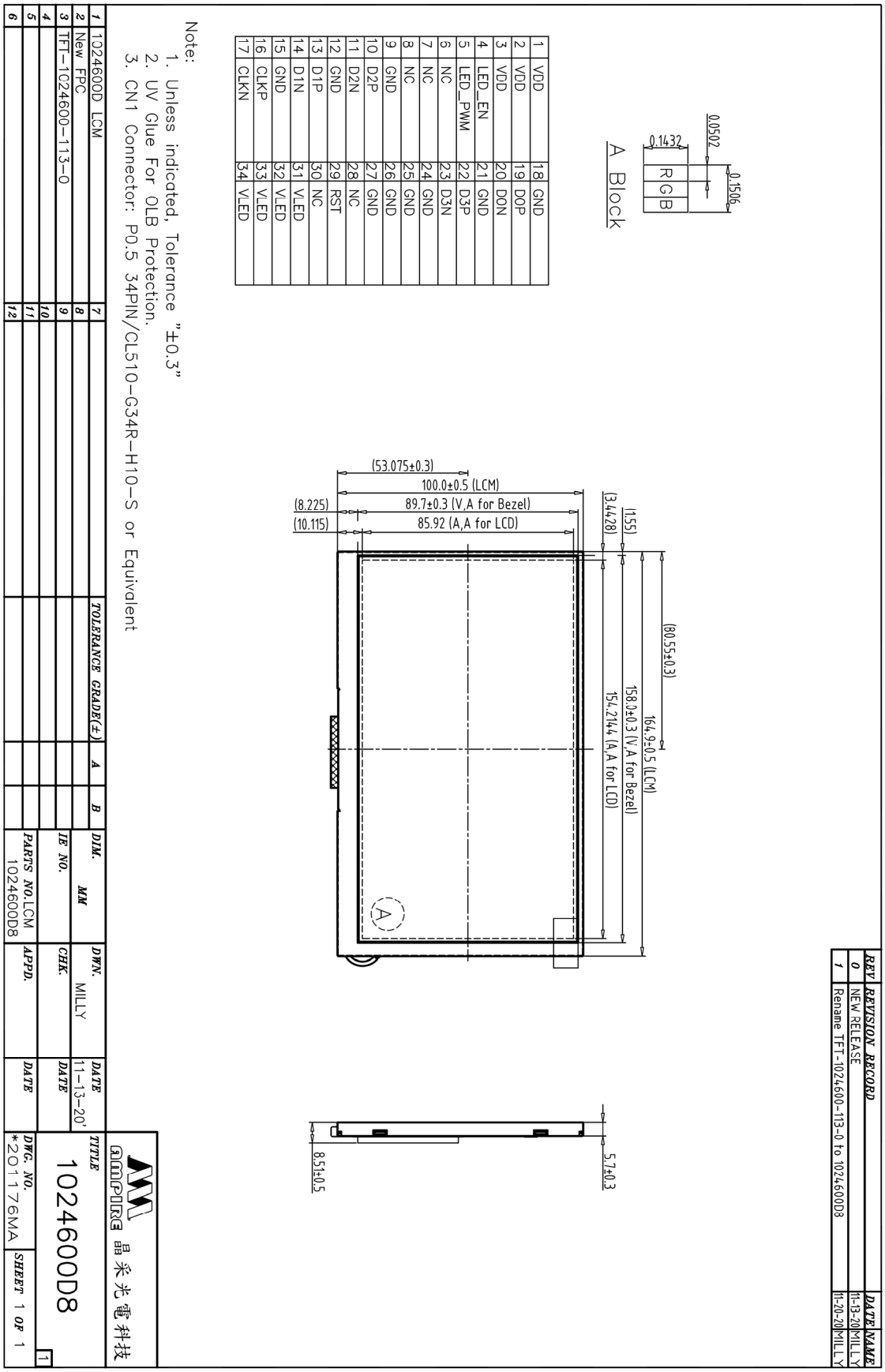
12.7 Others

(1) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

(2) Do not apply fixed pattern data signal to the LCD module as you are using the product.

(3) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.

13. Outline Dimension



1	VDD
2	VDD
3	VDD
4	LED_EN
5	LED_PWM
6	NC
7	NC
8	NC
9	GND
10	D2P
11	D2N
12	GND
13	D1P
14	D1N
15	GND
16	CLKP
17	CLKN
18	GND
19	D0P
20	D0N
21	GND
22	D3P
23	D3N
24	GND
25	GND
26	GND
27	GND
28	NC
29	RST
30	NC
31	V_LED
32	V_LED
33	V_LED
34	V_LED

REV.	REVISION RECORD	DATE	NAME
0	NEW RELEASE	11-13-20	MILLY
1	Rename TFT-1024600-113-0 to 1024600D8	11-20-20	MILLY

1	1024600D LCM	7	TOLERANCE GRADE(±)	A	B	DIM. MM	DWN. MILLY	DATE 11-13-20'	
2	New FPC	8				IE NO.	CHK.	DATE	
3	TFT-1024600-113-0	9				PARTS NO.LCM 1024600D8	APPD.	DATE	
4		10							
5		11							
6		12							

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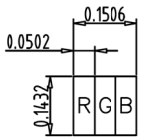
TITLE 1024600D8

DWG. NO. *2011176MA

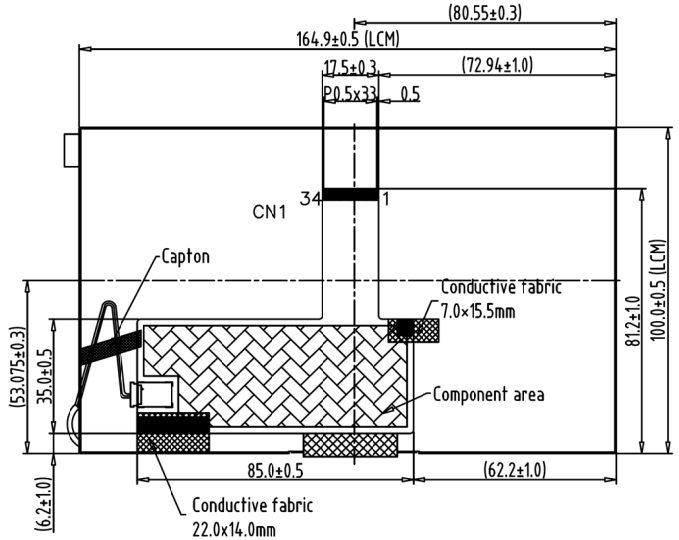
SHEET 1 OF 1

REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	01-31-24	MILLY

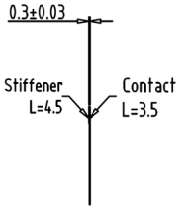


A Block

1	VDD	18	GND
2	VDD	19	DOP
3	VDD	20	DON
4	LED_EN	21	GND
5	LED_PWM	22	D3P
6	NC	23	D3N
7	NC	24	GND
8	NC	25	GND
9	GND	26	GND
10	D2P	27	GND
11	D2N	28	NC
12	GND	29	RST
13	D1P	30	NC
14	D1N	31	VLED
15	GND	32	VLED
16	CLKP	33	VLED
17	CLKN	34	VLED



Back View



Note:
1. Unless indicated, Tolerance "±0.3"
2. UV Glue For OLB Protection.
3. CN1 Connector: P0.5 34PIN/CL510-G34R-H10-S or Equivalent

1	1024600D8 LCM	7		TOLERANCE GRADE(±)	A	B	DIM. MM	DWN. MILLY	DATE 01-31-24'	TITLE 1024600D8-A
2	New FPC	8								
3		9					IE NO.	CHK.	DATE	
4		10								
5		11					PARTS NO. LCM-1 1024600D8-A	APPD.	DATE	DWG. NO. *240191MA / SHEET 1 OF 1
6		12								

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AMPIRE CO., LTD.

Date: 2025/05/26

14. Package

TBD