# Avnet MicroZed 7010/7020
# Revision G Errata
## V1.2
## 5 November 2020

# Table of Contents

# 1 Introduction

Thank you for your interest in the Avnet MicroZed System-On-Modules. Although Avnet has made every effort to ensure the highest possible quality, these kits and associated software are subject to the limitations described in this errata notification.

Be aware that any of the optional workarounds requiring physical modifications to the board are done at the User's own risk, and Avnet is not liable for poorly performed rework.

# 2 Identifying Affected Modules

The modules affected by these errata can be identified by the Revision of the MicroZed System-On-Module. The revision of the MicroZed System-On-Module can be found on the bottom side of the PCB board. The affected PCB boards are the MicroZed Revision G, identified as PCB assembly number "BD-Z7MB-Z7020-G REV-G" or "BD-Z7MB-Z7020I-G REV-G" or number "BD-Z7MB-Z7010-G REV-G" or "BD-Z7MB-Z7010I-G REV-G" with an embedded "PCB-G" also visible in the board etching.

Note: Unless explicitly stated in the errata, the errata will affect all MicroZed modules. Some errata below only affect specific MicroZed 7020 modules.

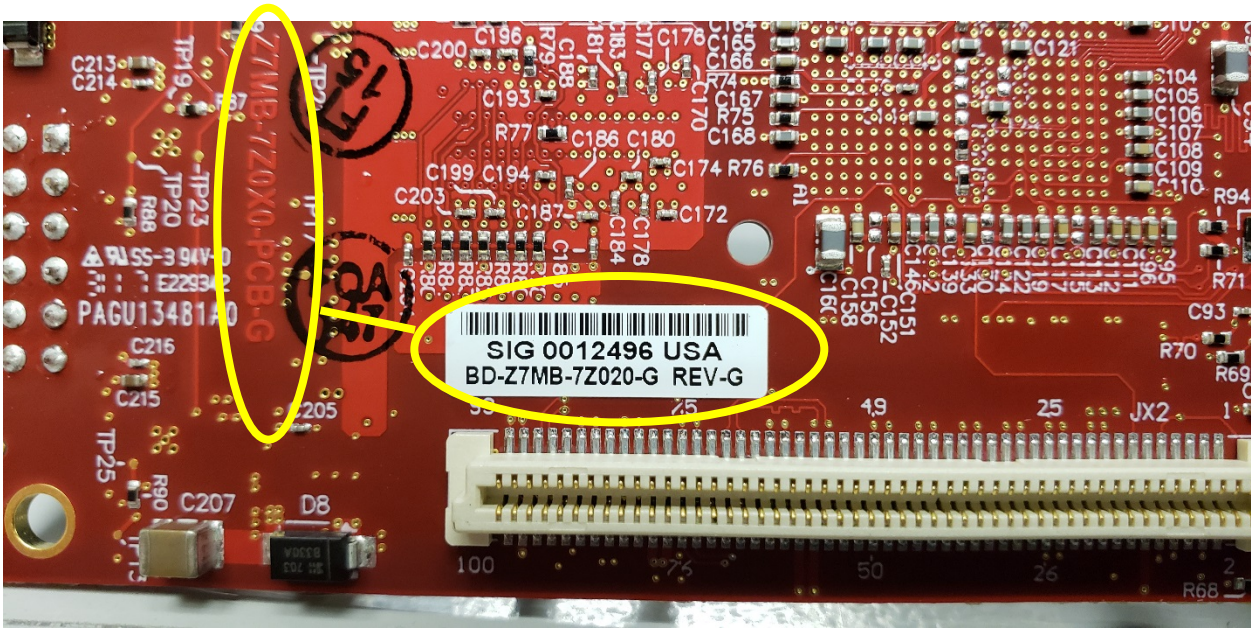


**Figure 1 – Identifying MicroZed Revision G**

# 3 Errata

## 3.1 PUDC_B Pull-up Populated with 0-ohm instead of 1K-ohm

### 3.1.1 Applications Affected

This issue will affect any MicroZed carrier board that makes use of signal JX1_LVDS_2_P, which is connected to JX1 Pin 17. This pin will have a short to VCCO_34 (JX1, Pins 78-80) once the MicroZed is plugged in.

Both the commercial and industrial temperature grade MicroZed 7020 Revision G models are affected by this issue.

Note: This issue was corrected before any MicroZed 7010 Revision G models were built.

- AES-Z7MB-7Z020-SOM-G
- AES-Z7MB-7Z020-SOM-I-G

Since none of the Avnet MicroZed Carrier boards use this I/O for active functionality, those Carriers are not affected.

### 3.1.2 Description

PUDC_B is a signal on the Zynq-7000 device that stands for “Pull-Ups During Configuration,” and it is active low. Since pull-ups during configuration can adversely affect I/Os that are strapped low, Avnet typically disables PUDC by adding a pull-up to the PUDC_B signal.

On MicroZed, the PUDC_B signal is in Bank 34 of the Zynq-7000, Pin U13 on component U9C on Sheet 6 of the schematic document. This pin is tied to schematic signal JX1_LVDS_2_P, which is also tied to resistor jumper JT4 and Micro Header JX1 Pin 17.

Resistor jumper JT4 is a 3-pad component that allows an 0402 resistor to be placed either in the 1-2 position or the 2-3 position. By default, this was supposed to be populated with a 1K-ohm resistor in the 1-2 position. Unfortunately, this was mistakenly populated with a 0-ohm resistor, thus shorting JX1_LVDS_2_P to power supply VCCO_34. This effectively disables PUDC, but it also makes this I/O unusable.

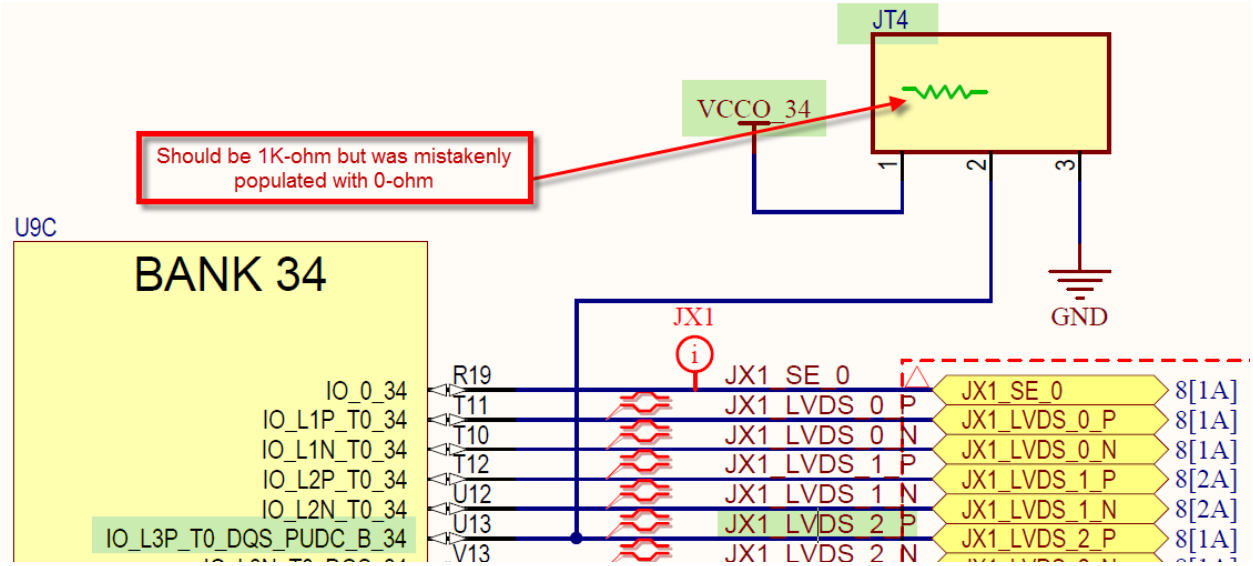


**Figure 2 – JT4 Pull-up Connected to PUDC_B, JX1_LVDS_2_P, and JX1-Pin17**

### 3.1.3 Workaround

If you are capable of completing the rework on your own, please contact customize@avnet.com to obtain a waiver before completing the work to avoid invalidating your warranty.

If you would like to return these boards to Avnet to complete this rework on affected boards that you already own, please contact us at customize@avnet.com.

If your application requires this specific IO for future MicroZed purchases, please contact customize@avnet.com to ensure any future product purchased will have the necessary changes.

To perform the rework yourself, perform the following steps:

1. Remove the resistor at position 1-2 of JT4.

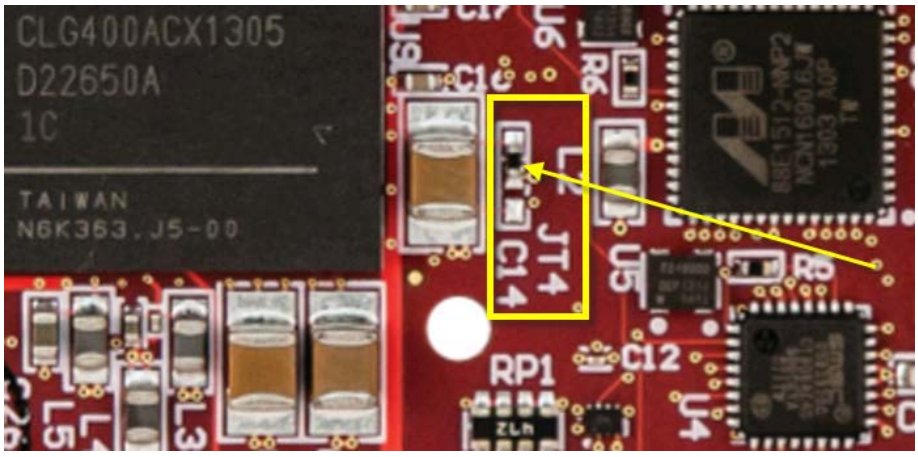


**Figure 3 – JT4 on MicroZed**

2. Solder a new, 0402 1K-ohm resistor to position 1-2 of JT4. A few suggestions are listed below.

    a. Panasonic Electronic Components ERJ-2RKF1001X

    b. Yageo AC0402FR-071KL

    c. Yageo RC0402FR-071KL

### 3.1.4 Identifying Repaired or New Boards

A repaired Revision G board that has this workaround in place will be identified with a blue mark on the bar code label as shown below:


**Figure 4 – Repaired MicroZed Rev G Board**

New Revision G boards with Revision Code G-03-03 or later will have a 2D bar code label like the one shown below. These boards do not have the issue.

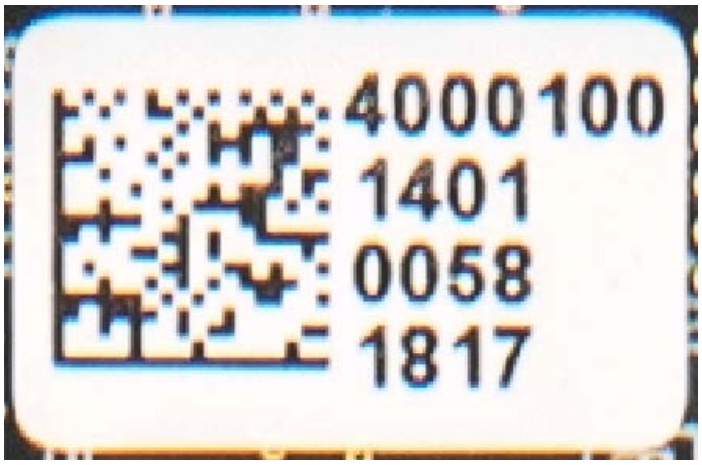


**Figure 5 – Example 2D Bar Code for Future Rev G MicroZed Boards**
**(Note: this is only an example bar code, not from MicroZed)**

## 3.2 User LED D3 Will Not Light When Driven

### 3.2.1 Applications Affected

The issue only affects a specific set of boards that were built at Contract Manufacturer MSC, with serial numbers starting with “MSC” and in the range shown in the table below:

| MicroZed Part Number | Starting Serial Number | Ending Serial Number |
|---|---|---|
| AES-Z7MB-7Z010-G | 1740000 | 1740459 |
| AES-Z7MB-7Z010I-G | 1750000 | 1750079 |
| AES-Z7MB-7Z020-G | 1760000 | 1760399 |
| AES-Z7MB-7Z020I-G | 1770000 | 1770079 |

Applications that control User LED D3 using PS MIO47 on pin B14 will not be able to light the LED.

### 3.2.2 Description

LED D3 was placed backwards during assembly and will therefore not operate properly. Once the LED is soldered in reverse position, it will operate correctly.

### 3.2.3 Workaround

If you are capable of completing the rework on your own, please contact customize@avnet.com to obtain a waiver before completing the work to avoid invalidating your warranty.

If you would like to return these boards to Avnet to complete this rework on affected boards that you already own, please contact us at customize@avnet.com.

### 3.2.4 Identifying Repaired or New Boards

A repaired Revision G board that has this workaround in place will be identified with a green mark on the bar code label as shown below. See 3.1 for an explanation regarding the blue mark on the right side.


**Figure 6 – Repaired MicroZed Rev G Board**

Any Revision G boards outside the ranges given in 3.2.1 will not exhibit the problem.

## 3.3 Custom Carrier Won't Power On, PG_1V8 / VCCIO_EN Voh-Min Is 1.2V

### 3.3.1 Applications Affected

Custom carriers that use a comparator expecting PG_1V8 / VCCIO_EN >= 1.4V (as was the case on Revisions F-05 and prior) will be affected as the PG_1V8 / VCCIO_EN Voh-Min on Revision G was modified to have a Voh-Min >= 1.2V, which is consistent with MicroZed Rev F-06 and PicoZed.
None of Avnet's MicroZed Carriers exhibit this problem.

### 3.3.2 Description

MicroZed carriers are required to monitor the PG_1V8 / VCCIO_EN (JX2.pin10) to properly sequence the bring-up of various power supplies, such as the I/O power supplies. This signal is driven on the MicroZed from U15.pin4 and is also affected by voltage divider R35 / R91.

On MicroZed Revisions F-05 and earlier, an issue was identified where this signal was affected by back feed voltage from the VTT regulator. Resistor R35 was changed from 1.0K to 1.5K on Revision F-06 to accommodate this other issue. Revision G maintained this 1.5K resistor for consistency.

The VTT back feed problem was corrected on Revision G, so R35 could be replaced with 1.0K-ohm without issue.

### 3.3.3 Workaround

It is recommended that users modify their comparator circuits to allow voltages as low as 1.2V to trigger an enable.

Users may also choose to modify R35 to 1.0K-ohm. It is possible for Avnet to build MicroZed Rev G with R35 at 1.0K-ohm as a custom part number with an MOQ. Please contact us at customize@avnet.com.

## 3.4 Ethernet Reset Duration

### 3.4.1 Applications Affected

Any application that would require the use of MicroZed Ethernet interface.

### 3.4.2 Description

Resistor/Capacitor circuit R106/C224 of the MicroZed 7010/7020 is affected by this erratum. The resistor/capacitor values that are placed do not meet the Ethernet reset requirement of 10ms that is required by the PHY. The current time required to release the Ethernet reset is on the order of 4.7 milliseconds.

### 3.4.3 Workaround

If the Ethernet reset duration significantly impacts operation in the end user application an option exist that will allow for proper operation of the Ethernet PHY. The option is to modify hardware to change the capacitor value of the resistor/capacitor combo that will allow for a time constant that is larger than the 10ms that is required by the PHY.

Recommended C224 capacitor value: 2.2uF (0402 package)

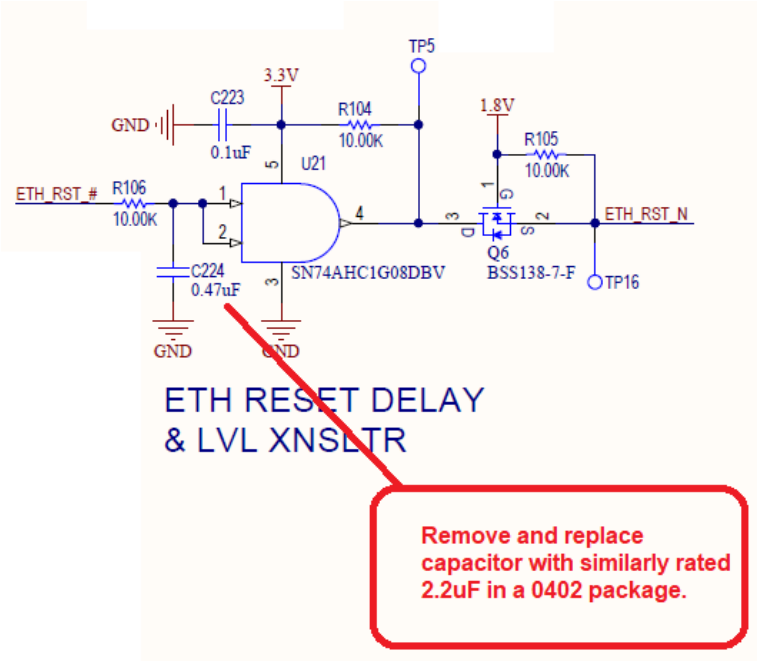


**Figure 7 – Ethernet Reset Capacitor for Proper Delay**

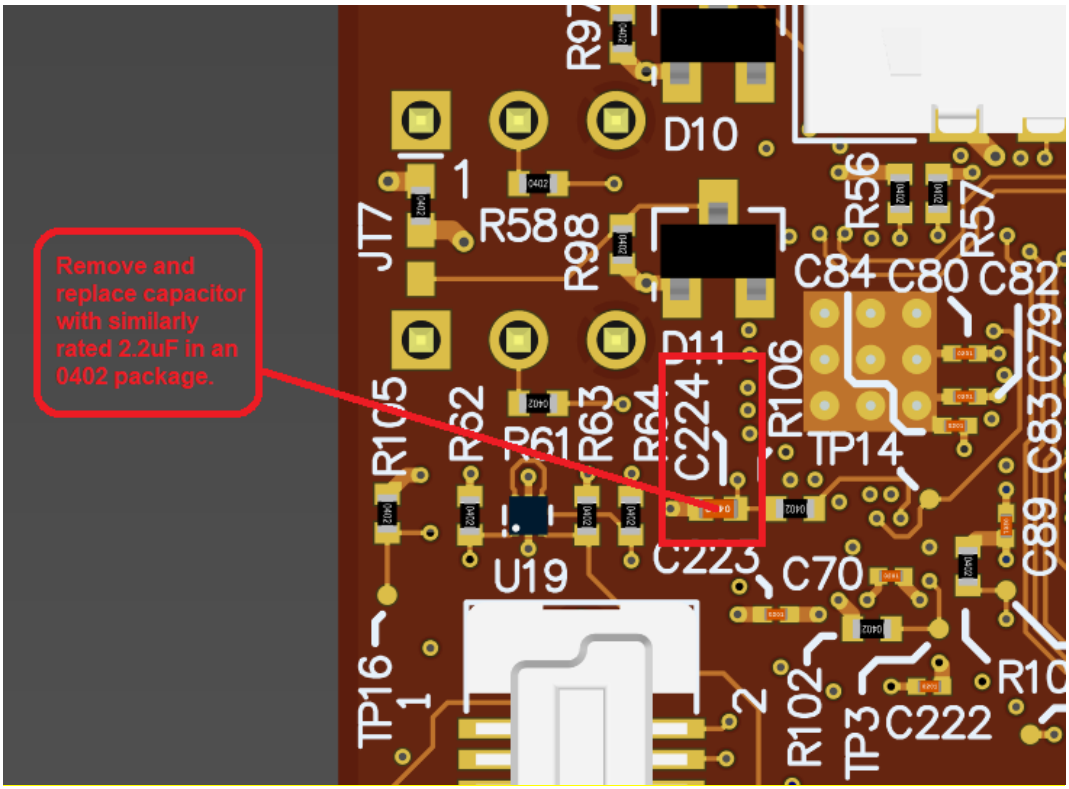


**Figure 8 – C224 Location on MicroZed**

If you are capable of completing the rework on your own, please contact customize@avnet.com to obtain a waiver before completing the work to avoid invalidating your warranty.

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If your application requires this specific errata modification for future MicroZed purchases, please contact customize@avnet.com to ensure any future product purchased will have the necessary changes.

## 3.5 Ethernet Reset Voltage Level

### 3.5.1 Applications Affected

Any application that would require the use of MicroZed Ethernet interface.

### 3.5.2 Description

Signal ETH_RST_# of the MicroZed 7010/7020 is affected by this erratum. This signal is the output of a translation circuit from 3.3V to 1.8V and enters the ethernet reset RC delay circuit described previously. The ETH_RST_# signal is the source for the RC time delay circuit used to implement the final ethernet reset to the PHY. The VIH (high-level input voltage) for the AND GATE IC, U21, that the delayed 1.8V ETH_RST_# signal drives has a minimum voltage of 2.1V which will not be achievable by the ETH_RST_# signal. This circuit relies on the 3.3V output pullup to bring the signal to a safe 3.3V level prior to being translated to 1.8V by the FET circuit prior to the PHY.

### 3.5.3 Workaround

If the Ethernet reset control impacts operation in the end user application a possible option exists that will allow for proper operation of the Ethernet PHY. The option is to modify hardware to dead bug resistor R106 to remove ETH_RST_# from the RC time delay circuit. Where the dead bug of resistor R106 occurs, signal PG_MODULE, TP15 in Figure 9 below, could be used to replace the ETH_RST_# signal which would put the proper voltage level on the ethernet reset RC time delay and translator circuits.

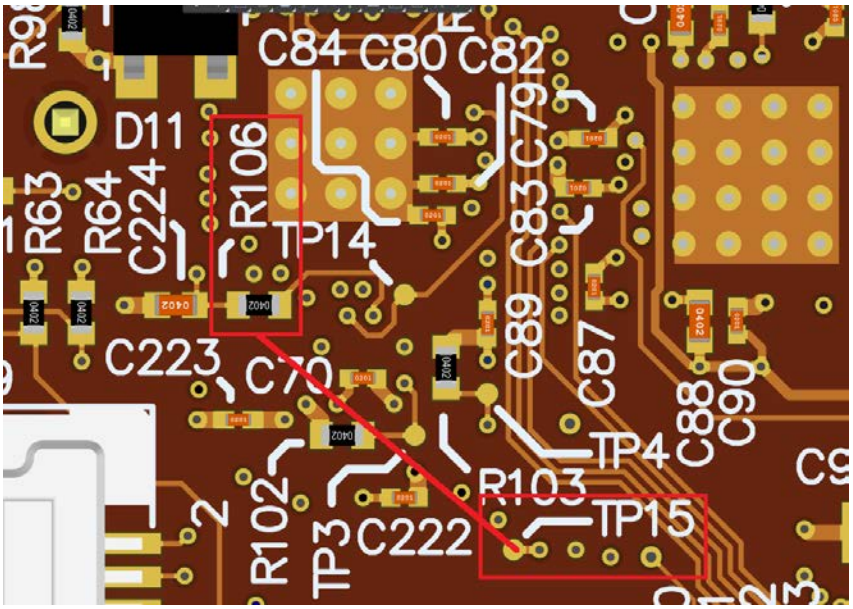


**Figure 9 – Ethernet Reset Proper Voltage Level on MicroZed**

This workaround should not be anticipated as a permanent solution. It is recommended that users migrate to MicroZed Revision H to avoid this voltage level issue if proper operation of the Ethernet PHY is needed.

If you are capable of completing the rework on your own, please contact customize@avnet.com to obtain a waiver before completing the work to avoid invalidating your warranty. If you would like to return these boards to Avnet to complete this rework on affected boards that you already own, please contact us at customize@avnet.com. If your application requires this specific errata modification for future MicroZed purchases, please contact customize@avnet.com to ensure any future product purchased will have the necessary changes.

## 3.6 QSPI Reset Voltage Level

### 3.6.1 Applications Affected

None - There have not been any adverse functionality reports regarding the on-board QSPI.

### 3.6.2 Description

QSPI pin A4 is RST#/RFU and is currently attached through a 0-ohm resistor to signal PS_SRST#. The QSPI is operated from a 3.3V power supply and concerns have been raised that the PS_SRST# signal is a 1.8V signal.

### 3.6.3 Workaround

Removing 0-ohm resistor R69 would allow the QSPI device to only use an internal pull-up resistor to control the reset of the device and eliminate the concern that a 1.8V signal was driving a 3.3V IO.

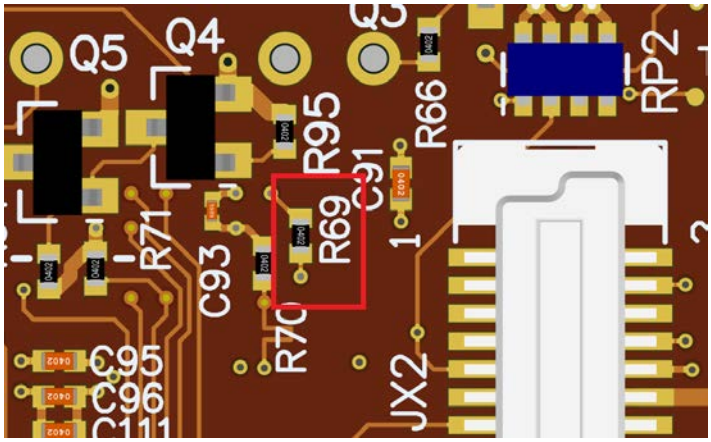


**Figure 10 – QSPI Reset Resistor R69 on MicroZed**

If you are capable of completing the rework on your own, please contact customize@avnet.com to obtain a waiver before completing the work to avoid invalidating your warranty.

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## 3.7 eFuse Integrity in MicroZed - Standalone Mode

### 3.7.1 Applications Affected

Any application where MicroZed is operated in standalone mode, ie – powered by USB whether from a PC or an AC to UBS brick.

### 3.7.2 Description

Under certain conditions, during power-on and power-off the integrity of the Zynq-7000 SoC PS eFUSE settings can be affected. Xilinx produced Answer Record AR# 65240 which is a design advisory for Zynq-7000 SoC covering power on and power off sequencing requirements for eFuse Integrity. Xilinx also updated sequencing requirements in their Zynq-7000 datasheets covering power on and power off sequencing for the Zynq-7000 series of devices.

Specifically, MicroZed when operated in standalone mode fails the power off test number 4 which is a test to see if PS_POR_B is held de-asserted ($V_{CCO\_MIO0}$) and the voltage ramp downs on $V_{CCPINT}$, $V_{CCPAUX}$ and $V_{CCO\_MIO0}$ are *monotonic* until at least one of the supplies reaches and stays below 0.40V, 0.70V and 0.90V respectively. During testing, in standalone mode, the MicroZed de-asserts and reasserts the PS_POR_B during power off and it has been shown that the PS_POR_B on reassertion occurs prior to some of the mentioned rails being below the presented levels. It has also been found that the PS_CLK signal is also still oscillating during this power off period.

If the eFuse integrity issues impacts module operation in standalone mode, possible modification options exist that will allow for proper operation resolving the issues potentially affecting eFuse integrity. The first modification is to tie PG_MODULE signal to the ENABLE pin of the PS_CLK oscillator. The second modification is to remove the TLV62130 power supplies on the module and replace with TLV62130A devices. The TLV62130A has a more robust Power Good signal which resolves the issues seen in standalone mode.

The modification to the PS_CLK oscillator is to tie PG_MODULE signal to PAD 2 of R100 (NETR100_2) in Figure 11.

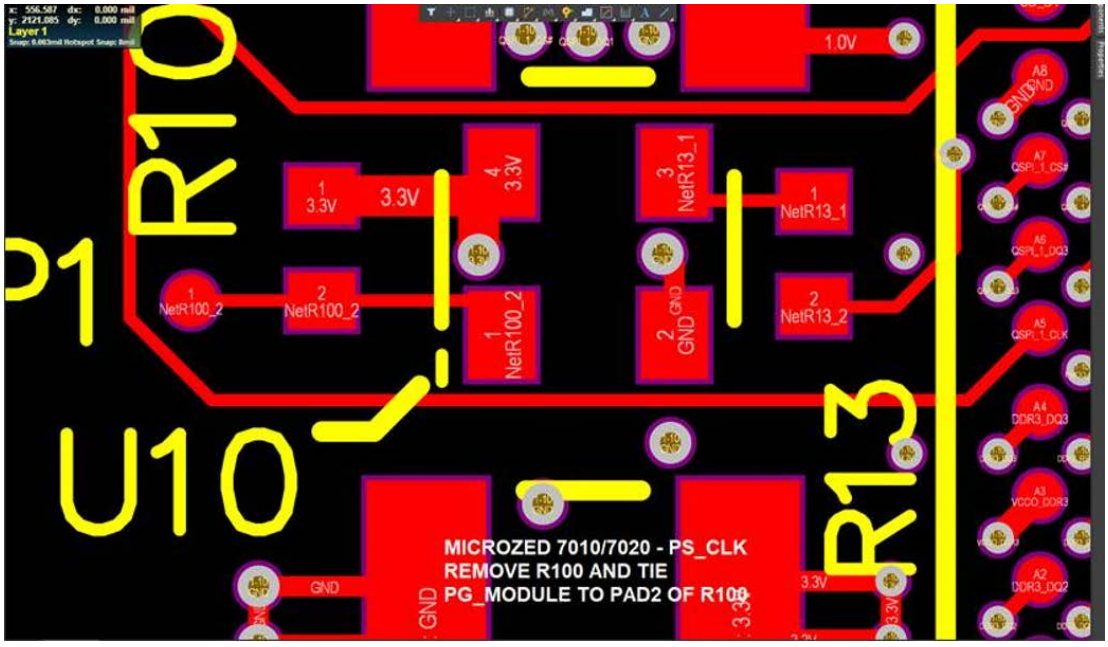


**Figure 11 – OSC Enable Resistor R100 on MicroZed**

Figure 12 is the location of PG_MODULE that can be utilized in the OSC Enable modification.

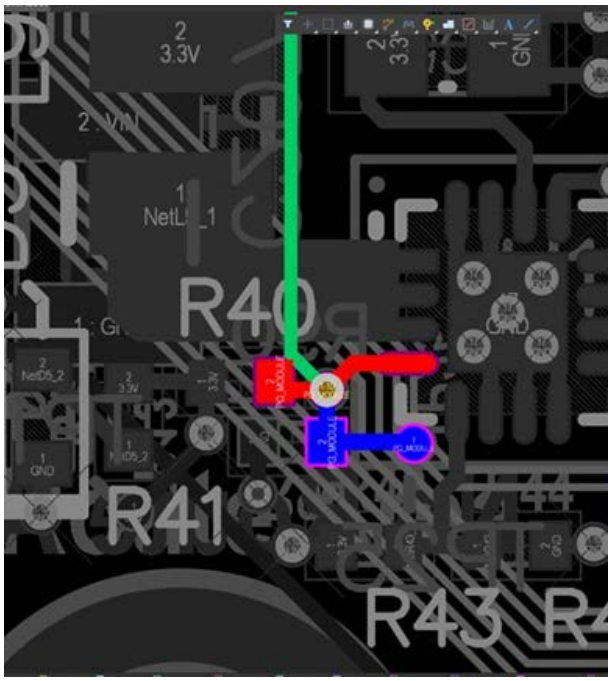


**Figure 12 – PG_MODULE location on MicroZed**

These workarounds should not be anticipated as a permanent solution. It is recommended that users needing to operate in standalone mode migrate to MicroZed Revision H to avoid this potential eFuse integrity issue.

If you are capable of completing the rework on your own, please contact customize@avnet.com to obtain a waiver before completing the work to avoid invalidating your warranty.

If you would like to return these boards to Avnet to complete this rework on affected boards that you already own, please contact us at customize@avnet.com.

If your application requires this specific errata modification for future MicroZed purchases, please contact customize@avnet.com to ensure any future product purchased will have the necessary changes.

# 4 New Erratum

Any new erratum found will be posted to the MicroZed website forum:

http://avnet.me/microzed_forum

# 5 Additional Support

For additional support, please review the discussions and post your questions to the MicroZed Forums at:

http://avnet.me/microzed_forum

You can also contact your local Avnet FAE.

# 6 Revision History

| Date | Version | Revision |
|---|---|---|
| 26 Jun 2018 | 1.0 | Added Item 3.1 PUDC_B Pull-up Populated with 0-ohm instead of 1K-ohm |
| 02 Mar 2019 | 1.1 | Added Item 3.2 User LED D3 Will Not Light When Driven.<br>Added Item 3.3 Custom Carrier Won't Power On, PG_1V8 / VCCIO_EN Voh-Min Is 1.2V |
| 5 Nov 2020 | 1.2 | Added Item 3.4 Ethernet Reset Duration<br>Added Item 3.5 Ethernet Reset Voltage Level<br>Added Item 3.6 QSPI Reset Voltage Level<br>Added Item 3.7 eFuse Integrity |