

# Model Name: P366IVN02.0

Issue Date: 2024/09/20

- ( ) Preliminary Specifications
- (\*) Final Specifications

Customer Signature	Date	AUO Display Plus	Date
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## Record of Revision

[illegible]

### 1. General Description

This specification applies to the 36.6 inch Color TFT-LCD Module P366IVN02.0. This LCD module has a TFT active matrix type liquid crystal panel 1920x290 pixels, and diagonal size of 36.6 inch. This module supports 1920x290 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

P366IVN02.0 has been designed to apply the 8-bit 2 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important. Special materials applied into this model is:

1. Liquid crystal: High Tni LC (110℃) or Advanced wide temperature LC(-40℃~110℃)
2. Polarizer: Wide temperature polarizer (95℃)

\* General Information

Items	Specification	Unit	Note
Active Screen Size	36.6	inch	
Display Area	919.296(H) x 138.852(V)	mm	
Outline Dimension	951.3(H) x 170.8(V) x 28.8 (D)	mm	D: front bezel to DB cover
Driver Element	a-Si TFT active matrix		
Display Colors	8 bit (16.7 million)	Colors	
Number of Pixels	1920x290	Pixel	
Pixel Pitch	0.4788 (H) x 0.4788 (W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze = 25%
Rotate Function	Unachievable		Note 1
Display Orientation	Portrait/Landscape Enabled		Note 2
Sunglasses Readability	Portrait mode or Landscape Mode		Note 3
Operating Time	24/7		See Chapter 11.3 for details
Frame Rate	60	Hz	See Chapter 5.1 for details
LED MTTF	50K	hours	See Chapter 6.1 for details

Note 1: Rotate Function refers to LCD display could be able to rotate. This function does not work in this model.

Note 2:

- (1) Landscape Mode: The default placement is T-Con Side on the lower side and the image is shown upright via viewing from the front.
- (2) Portrait Mode: The default placement is that T-Con side has to be placed on the left side via viewing from the front.

已註解 [a1]: 確認 model 是 8-bit or 10-bit

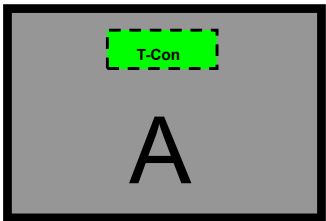
已註解 [P2]: 表面處理不同，硬度也會不同，請確認後再 update,請點開右下角白框參考  
若為圖偏，敘述為: "Low Reflection, QWP", Refelctance<2%

Type

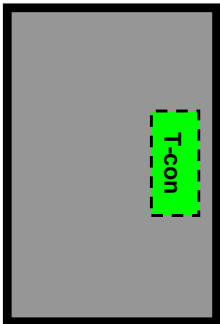
已註解 [H呂3R2]:  
2024/05/23 被要求改 AG25%但產品實際為 AG28%

已註解 [eva4]: Portrait mode 有對應的 RA 項目,需完成驗證才能宣稱該機種支援 Portrait mode, T-con 位置圖請 EE RD 提供, 與機構 RD 確認方向

Landscape (Front view)



Portrait (Front view)

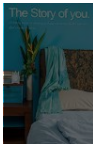


**Note 3:**  
The image can be seen via polarized sunglasses while this panel is placed in landscape or portrait mode.

Display Orientation:



Landscape



Portrait



Polarized Sunglasses

已註解 [TH黃5]: 高亮( $\geq 1500\text{nit}$ ) 線偏機種  
請依照產品的偏光片角度選擇圖示。

## 2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V <sub>DD</sub>	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	V <sub>in</sub>	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	-25	+60	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-25	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

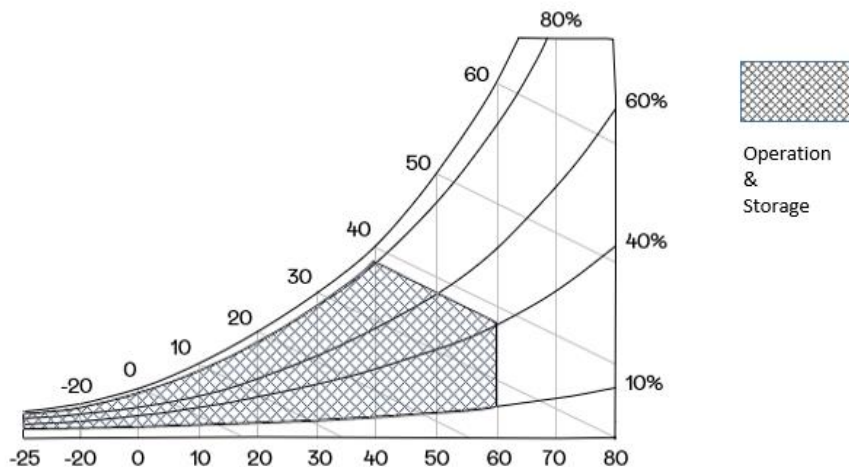
Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40 °C or less. At temperatures greater than 40 °C, the wet bulb temperature must not exceed 39 °C.

Note 3: Within the specified operating temperature range, the panel surface temperature (PST) must not exceed this value.

已註解 [B6]: 需 Pass -20~60 的 RA items 方可將操作溫度改-20~60  
溫度, 濕度圖須選對應圖(如下)

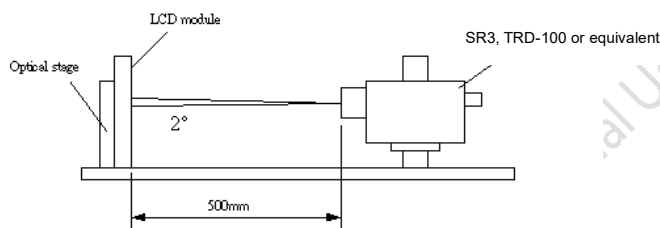


已註解 [a7]: -20~60 度 請選此圖,請自行拉對角放大

### 3. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are at an approximate distance 500 mm from the LCD surface at a viewing angle of  $\varphi$  and  $\theta$  equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	4200	5000	--		1
Surface Luminance (White)		L <sub>WH</sub>	1320	1650	--	cd/m <sup>2</sup>	2
Luminance Variation		$\Delta$ <sub>WHITE(9P)</sub>	--	--	1.33		3
Response Time (G to G)		T <sub>Y</sub>	--	8	16	ms	4
Color Gamut		NTSC		50		%	
Color Coordinates							
	Red	R <sub>X</sub>	Typ.-0.03	0.610	Typ.+0.03		
		R <sub>Y</sub>		0.331			
	Green	G <sub>X</sub>		0.335			
		G <sub>Y</sub>		0.566			
	Blue	B <sub>X</sub>		0.158			
		B <sub>Y</sub>		0.106			
	White	W <sub>X</sub>		0.313			
		W <sub>Y</sub>		0.329			
Viewing Angle							5
	x axis, right( $\varphi=0^\circ$ )	$\theta_r$	85	89	--	degree	
	x axis, left( $\varphi=180^\circ$ )	$\theta_l$	85	89	--	degree	
	y axis, up( $\varphi=90^\circ$ )	$\theta_u$	85	89	--	degree	
	y axis, down ( $\varphi=270^\circ$ )	$\theta_d$	85	89	--	degree	

Note:

1. Contrast Ratio (CR) is defined mathematically as:

已註解 [H8]: 2024/05/23 被要求改 5000,但 MRS 是提報 4000

已註解 [P9]: RT:  
60Hz: Typ 8, Max 16  
120/240Hz: Typ 6, max 14

已註解 [B10]: 標準品選用 NTSC, 若為 NTSC 50%則改寫成 sRGB 72%

已註解 [P11]: Curve Module should change view angle value in x axis

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{\text{on5}}}{\text{Surface Luminance of } L_{\text{off5}}}$$

- Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. LED current  $I_F$  = typical value (without driver board), LED input  $V_{DDB}$  = 24V,  $I_{DDB}$  = Typical value (with driver board),  $L_{WH} = L_{on5}$  where  $L_{on5}$  is the luminance with all pixels displaying white at center 5 location.
- The variation in surface luminance,  $\delta_{\text{WHITE}}$  is defined (center of Screen) as:  

$$\delta_{\text{WHITE(9P)}} = \frac{\text{Maximum}(L_{on1}, L_{on2}, \dots, L_{on9})}{\text{Minimum}(L_{on1}, L_{on2}, \dots, L_{on9})}$$
- Response time  $T_V$  is the average time required for display transition by switching the input signal for five luminance ratio (0%, 25%, 50%, 75%, 100% brightness matrix) and is based on [Frame rate = 60Hz] to optimize.

已註解 [P12]: Here frame rate refers to display frame rate. For MEMC (60 Hz in 120Hz out) model, frame rate is 120Hz

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

$T_V$  is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray(bright) " and "any level of gray(dark)".

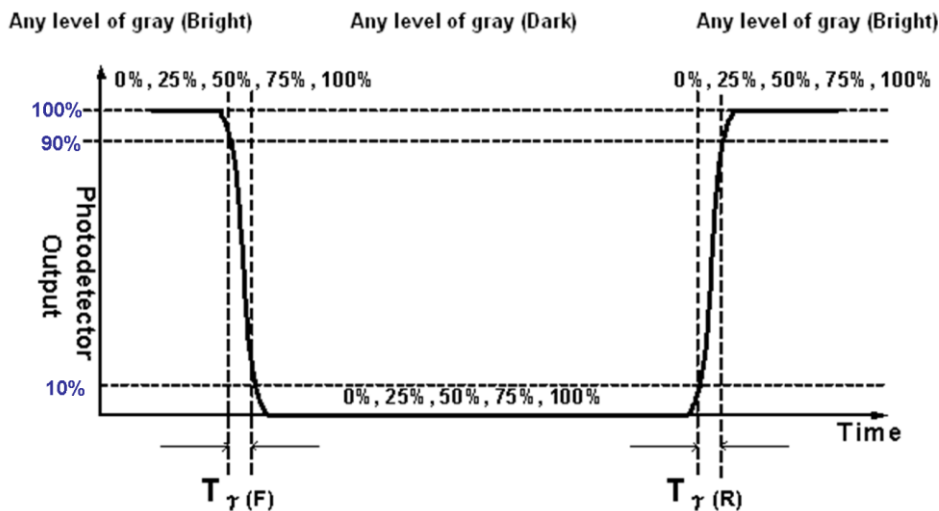
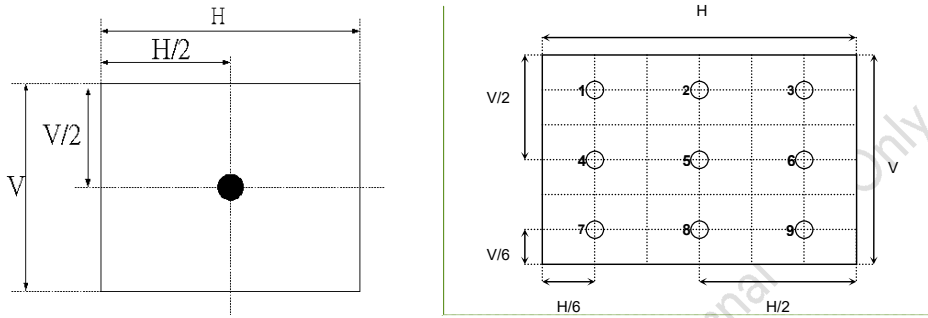


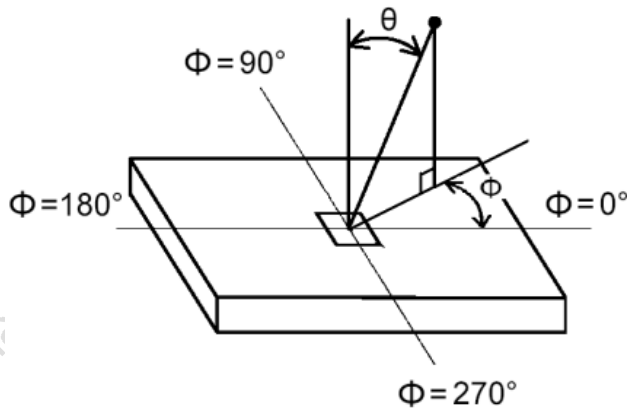


FIG. 2 Luminance



5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG3.

FIG.3 Viewing Angle



已註解 [P13]:

Standard: H/6, V/6

SEC model: H/9, V/9

Tartan: 依照實際量測手法標示

## 4. Interface Specification

### 4.1 Input power

The P3661VN02.0 module requires power inputs which are employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item	Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage	$V_{DD}$	10.8	12	13.2	V	1
Power Supply Input Current	$I_{DD}$	-	0.22	0.26	A	2
		-	0.34	0.41	A	
Power Consumption	$P_C$	-	2.63	3.15	Watt	
		-	4.10	4.92	Watt	
Inrush Current	$I_{RUSH}$	--	--	2.8	A	3

**Note1.** The ripple voltage should be fewer than 5% of VDD.

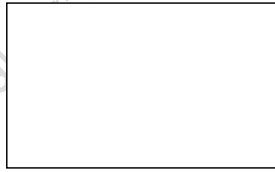
**Note2.** Test Condition:

- (1)  $V_{DD} = 12.0V$ , (2)  $F_v = 60Hz$ , (3)  $F_{clk} = 74.25MHz$ , (4) Temperature = 25 °C  
(5) Power dissipation check pattern. (Only for power design)

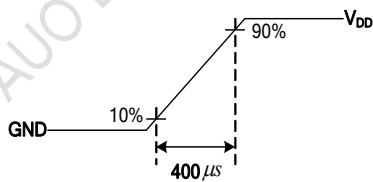
a. Black pattern



b. White pattern



**Note3.** Measurement condition : Rising time = 400us

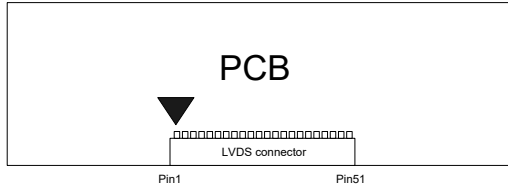


## 4.2 Input Connection

■ LCD connector: JAE SJ11346-FI-RTE51SZ-HF / P-Two 187059-5122 / Starconn 115E51-0000RA-M3-R

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	N.C.	No connection	2	26	N.C.	No connection	2
2	N.C.	No connection	2	27	N.C.	No connection	2
3	N.C.	No connection	2	28	CH2_Y0-	LVDS Channel 2, Signal 0-	
4	N.C.	No connection	2	29	CH2_Y0+	LVDS Channel 2, Signal 0+	
5	N.C.	No connection	2	30	CH2_Y1-	LVDS Channel 2, Signal 1-	
6	N.C.	No connection	2	31	CH2_Y1+	LVDS Channel 2, Signal 1+	
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	3	32	CH2_Y2-	LVDS Channel 2, Signal 2-	
8	N.C.	No connection	2	33	CH2_Y2+	LVDS Channel 2, Signal 2+	
9	N.C.	No connection	2	34	GND	Ground	
10	N.C.	No connection	2	35	CH2_CLK-	LVDS Channel 2, Clock -	
11	GND	Ground		36	CH2_CLK+	LVDS Channel 2, Clock +	
12	CH1_Y0-	LVDS Channel 1, Signal 0-		37	GND	Ground	
13	CH1_Y0+	LVDS Channel 1, Signal 0+		38	CH2_Y3-	LVDS Channel 2, Signal 3-	
14	CH1_Y1-	LVDS Channel 1, Signal 1-		39	CH2_Y3+	LVDS Channel 2, Signal 3+	
15	CH1_Y1+	LVDS Channel 1, Signal 1+		40	N.C.	No connection	2
16	CH1_Y2-	LVDS Channel 1, Signal 2-		41	N.C.	No connection	2
17	CH1_Y2+	LVDS Channel 1, Signal 2+		42	N.C.	No connection	2
18	GND	Ground		43	N.C.	No connection	2
19	CH1_CLK-	LVDS Channel 1, Clock -		44	GND	Ground	
20	CH1_CLK+	LVDS Channel 1, Clock +		45	GND	Ground	
21	GND	Ground		46	GND	Ground	
22	CH1_Y3-	LVDS Channel 1, Signal 3-		47	N.C.	No connection	2
23	CH1_Y3+	LVDS Channel 1, Signal 3+		48	V <sub>DD</sub>	Power Supply, +12V DC Regulated	
24	N.C.	No connection	2	49	V <sub>DD</sub>	Power Supply, +12V DC Regulated	
25	N.C.	No connection	2	50	V <sub>DD</sub>	Power Supply, +12V DC Regulated	
				51	V <sub>DD</sub>	Power Supply, +12V DC Regulated	

**Note1.** Pin number start from the left side as the following figure.

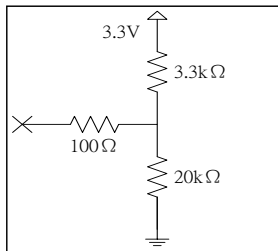


**Note2.** Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

**Note3.** LVDS data format selection

LVDS_SEL	Mode
H or OPEN	NS
L	Jeida

**Input equivalent impedance of LVDE\_SEL pin**



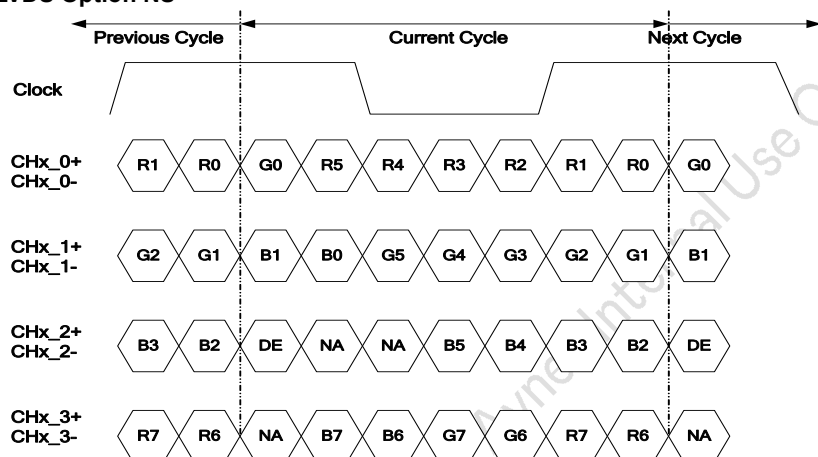
### 4.3 Input Data Format

#### 4.3.1 LVDS color data mapping

已註解 [P14]: 10 bit condition, 若有變動請參閱 EE 公版 SPEC

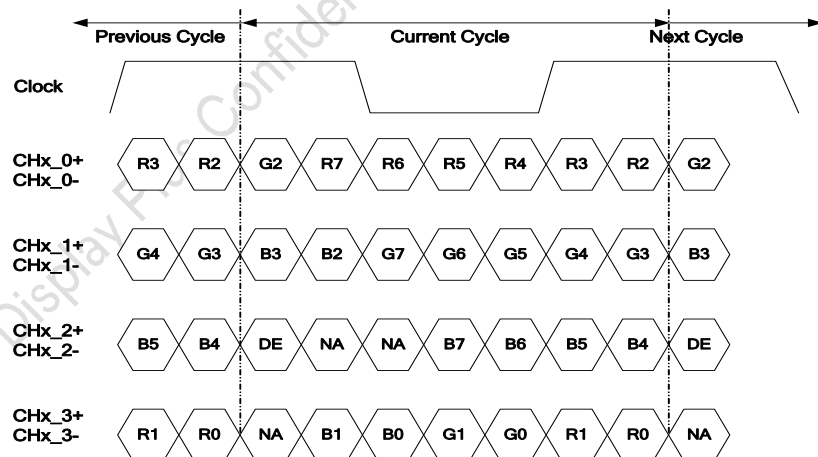
#### LVDS Option for 8bit

##### ■ LVDS Option NS



Note: x = 1, 2, 3, 4...

##### ■ LVDS Option JEIDA



Note: x = 1, 2, 3, 4...

#### 4.3.2 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

#### COLOR DATA REFERENCE

8bit

已註解 [P15]:

- 1.8bit
- 2.10bit (8+FRC)
- 3.8 or 10 bit (bit selectable)

已註解 [B16]: 10bit 機種請刪除此表

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB				LSB				MSB				LSB				MSB				LSB			
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	----																								
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	----																								
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	----																								
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

## 5. Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

已註解 [P17]: 5.1.1.1表格內容為  
1920x1080\_60Hz, AUO-12309,數值, 若有變動  
請參照 EE 公版 spec 或與 EE RD 確認

### 5.1 Input Timing

#### 5.1.1. Timing table

Timing Table (DE only Mode)

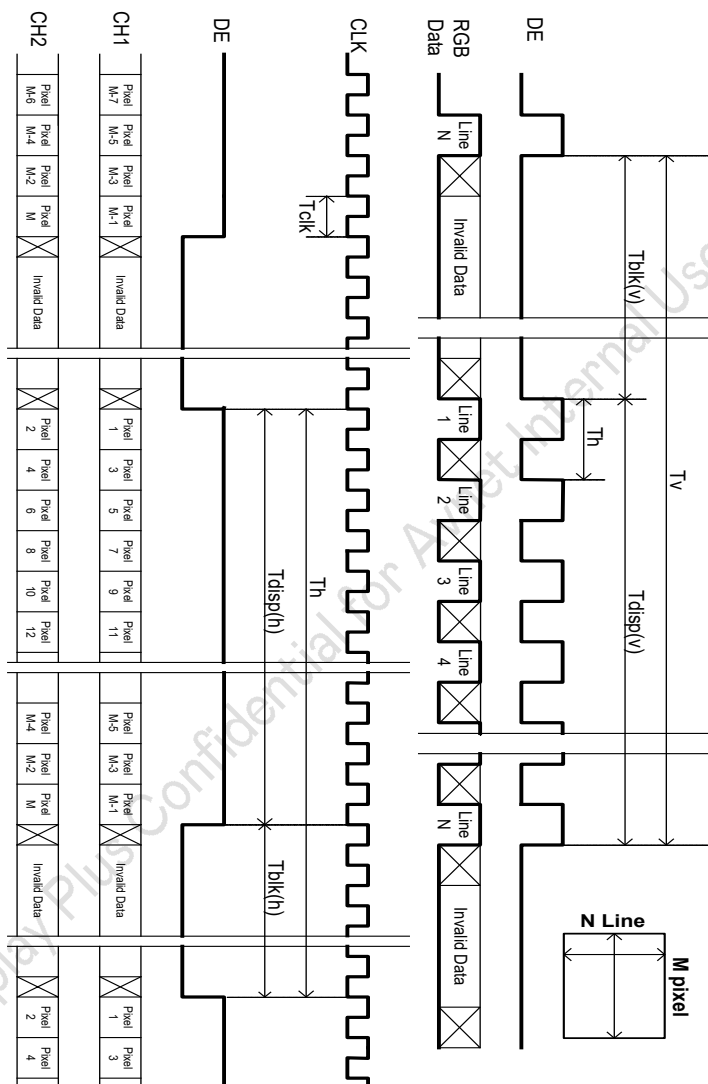
Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1120	1125	1480	Th
	Active	Tdisp (v)	1080			Th
	Blanking	Tblk (v)	40	45	400	Th
Horizontal Section	Period	Th	1060	1100	1325	Tclk
	Active	Tdisp (h)	960			Tclk
	Blanking	Tblk (h)	100	140	365	Tclk
Clock	Frequency	Fclk=1/Tclk	53	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz

Notes:

- (1) Display position is specific by the rise of DE signal only.  
Horizontal display position is specified by the rising edge of 1<sup>st</sup> DCLK after the rise of 1<sup>st</sup> DE, is displayed on the left edge of the screen.
- (2) Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1<sup>st</sup> data corresponding to one horizontal line after the rise of 1<sup>st</sup> DE is displayed at the top line of screen.
- (3) If a period of DE "High" is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.
- (4) The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.

### 5.1.2. Signal Timing Waveform

已註解 [P18]: 與 EE RD 確認後選擇使用的 wave form

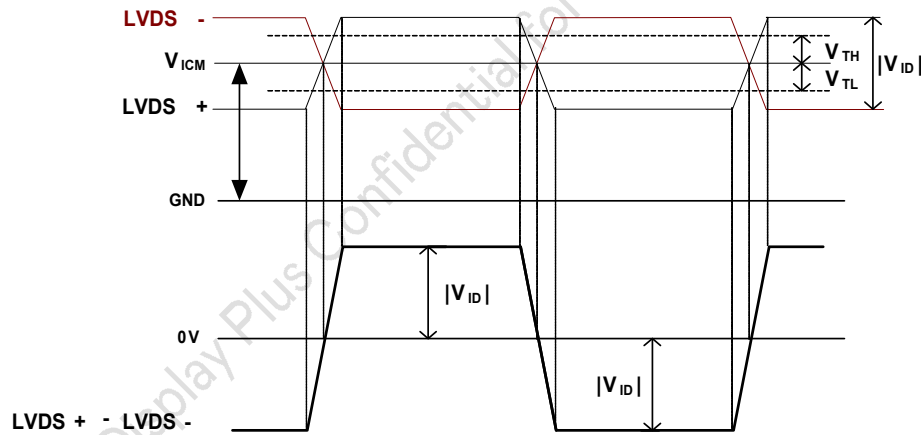




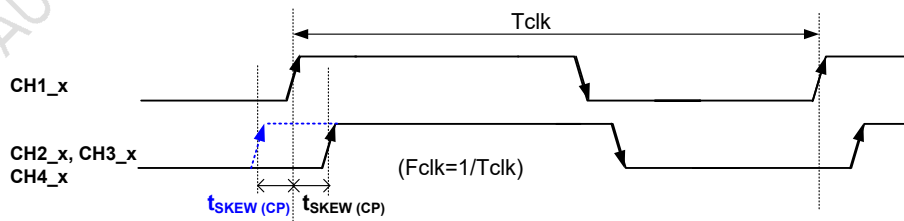
## 5.2 Input interface characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Differential Voltage	V <sub>ID</sub>	100	400	600	mV <sub>DC</sub>	1
	Differential Input High Threshold Voltage	V <sub>TH</sub>	--	--	+100	mV <sub>DC</sub>	1
	Differential Input Low Threshold Voltage	V <sub>TL</sub>	-100	--	--	mV <sub>DC</sub>	1
	Input Common Mode Voltage	V <sub>ICM</sub>	1.1	1.25	1.4	V <sub>DC</sub>	1
	Input Channel Pair Skew Margin	t <sub>SKEW (CP)</sub>	-500	--	+500	ps	2
	Input Channel Pair Skew Margin (only for M'Star MST7428BB)	t <sub>SKEW (CP)</sub>	-400	--	+400	ps	2
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	3
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	3
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	-0.4 -0.5	-- --	0.4 0.5	ns	8

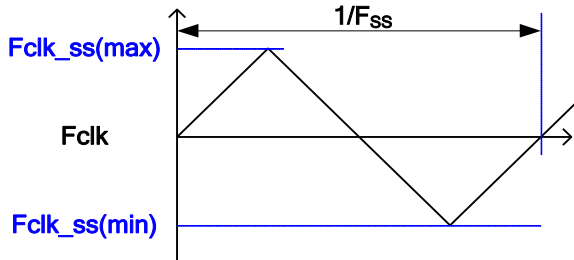
Note1.  $V_{ICM} = 1.25V$



Note2. Input Channel Pair Skew Margin

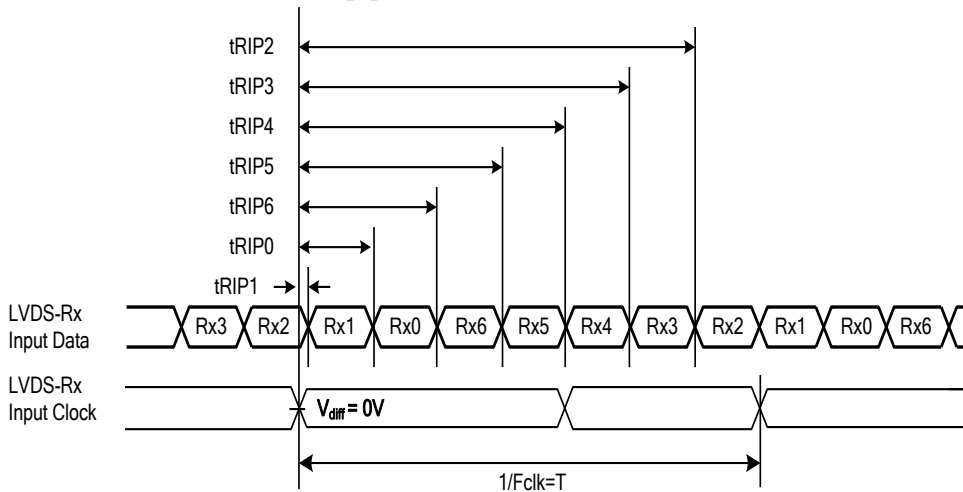


Note3. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.

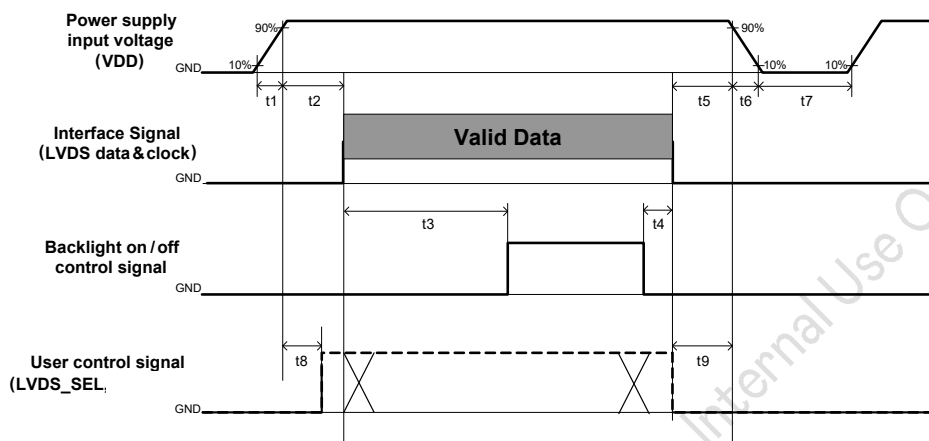


Note4. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	$T=1/F_{clk}$
Input Data Position0	tRIP1	- tRMG	0	tRMG	ns	
Input Data Position1	tRIP0	$T/7- tRMG $	$T/7$	$T/7+ tRMG $	ns	
Input Data Position2	tRIP6	$2T/7- tRMG $	$2T/7$	$2T/7+ tRMG $	ns	
Input Data Position3	tRIP5	$3T/7- tRMG $	$3T/7$	$3T/7+ tRMG $	ns	
Input Data Position4	tRIP4	$4T/7- tRMG $	$4T/7$	$4T/7+ tRMG $	ns	
Input Data Position5	tRIP3	$5T/7- tRMG $	$5T/7$	$5T/7+ tRMG $	ns	
Input Data Position6	tRIP2	$6T/7- tRMG $	$6T/7$	$6T/7+ tRMG $	ns	



### 5.3 Power Sequence for LCD



Parameter	Min.	Typ.	Max	Unit
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	400	---	---	ms
t4	0 <sup>*1</sup>	---	---	ms
t5	0	---	---	ms
t6	---	---	--- <sup>*2</sup>	ms
t7	1000 <sup>*3</sup>	---	---	ms
T8	20 <sup>*4</sup>	---	50	ms
T9	0	---	---	ms

Note :

- (1) t4=0 : concern for residual pattern before BLU turn off.
- (2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
- (3) t7 : When the power supply input voltage(VDD) is off, be sure to pull down the valid and invalid data to 0V.
- (4) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible

已註解 [P19]: 表格內容為

1920x1080\_50Hz/60Hz\_AUO-12411K02, 若為其他規格  
請參閱 EE 公版 spec 或與 EE RD 確認

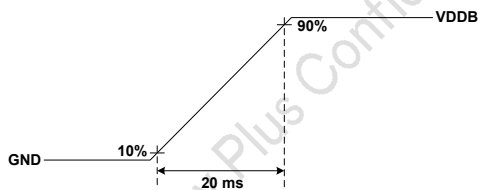
## 6. Backlight Specification

### 6.1 Electrical specification

	Item	Symbol	Condition	Min	Typ	Max	Unit	Note
1	Power Supply Input Voltage	V <sub>DDB</sub>	-	22.8	24	25.2	V	-
2	Power Supply Input Current	I <sub>DDB</sub>	V <sub>DDB</sub> =24V	-	1.53	1.68	A	1
3	Power Consumption	P <sub>DDB</sub>	V <sub>DDB</sub> =24V	-	36.6	40.3	Watt	1
4	Inrush Current	I <sub>RUSH</sub>	V <sub>DDB</sub> =24V	-	-	4.0	A	2
5	Control signal voltage	V <sub>Signal</sub>	V <sub>DDB</sub> =24V	2	-	3.6	V	-
				0	-	0.8		3
6	Control signal current	I <sub>Signal</sub>	V <sub>DDB</sub> =24V	-	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_EPWM	V <sub>DDB</sub> =24V	0	-	100	%	4
8	External PWM Frequency	F_EPWM	V <sub>DDB</sub> =24V	120	-	960	Hz	4
9	Input Impedance	R <sub>in</sub>	V <sub>DDB</sub> =24V	300			Kohm	-
10	LED MTTF	LTLED	-		50,000	-	Hr	5, 6

**Note 1:** Dimming ratio= 100%, (Ta=25±5°C, Turn on for 45minutes)

**Note 2:** MAX input current while DB turn on, measurement condition V<sub>DDB</sub> rising time=20ms(V<sub>DDB</sub>: 10%~90%)



**Note 3:** When BLU off (V<sub>DDB</sub> = 24V, V<sub>BLON</sub> = 0V), I<sub>DDB</sub> (max) = 0.1A

**Note 4:** Less than 5% dimming control is functional well and no backlight shutdown happened

**Note 5:** LED MTTF is defined as the time which luminance of LED is 50% compared to its original value.

[Operating condition: Continuous operating at Ta = 25±2°C, for single LED only]

**Note6:** MTTF is a reference index, it is not representative of warranty.

已註解 [P20]: 本章節為有提供 Driver board 的模組使用. 詳細設定參考 EE Spec, 若沒提供 driver board 請用 Without Driver Board 版本  
本章節內容為 normal BLU, 若有其它 function (scanning, boosting...)請參考 EE 公版 SPEC 或與 RD 確認

## 6.2 Input Pin Assignment

The module requires 1 power input .

LED Driver board connector:

CI0114M1HRL-NH(CviLux) or equivalent

### CI0114M1HRL-NH(CviLux)

Pin	Symbol	Description	Note
1	VDDDB	Power Supply Input Voltage	
2	VDDDB	Power Supply Input Voltage	
3	VDDDB	Power Supply Input Voltage	
4	VDDDB	Power Supply Input Voltage	
5	VDDDB	Power Supply Input Voltage	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No connection	3
12	VBLON	BLU On-Off control:	1,2
13	N.C.	No connection	3
14	PDIM	External PWM	1,4

#### Note1. input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.8	V

#### Note2. VBLON

Mode selection

VBLON	Note
H or OPEN	BL On
L	BL Off

**Note3.** Please leave this pin unoccupied. It cannot be connected by any signal (Low/GND/High).

**Note4. PDIM**

PWM Dimming range:



External PWM function dimming ratio 0%~100%, Judge condition as below:

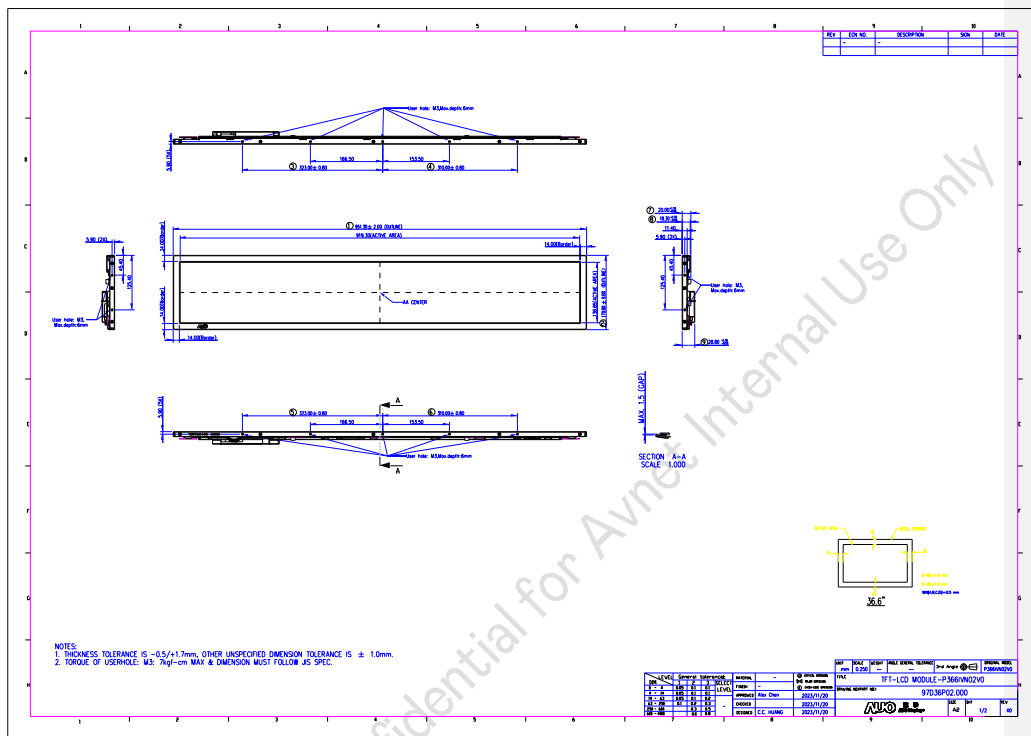
- (1) Backlight module must be lighted ON normally.
- (2) All protection function must work normally.
- (3) Uniformity and flicker could be guaranteed at External PWM function dimming ratio 5%~100%

## 7. Mechanical Characteristics

The contents provide general mechanical characteristics for the model P366IVN02.0. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Item		Dimension	Unit	Note
Outline Dimension	Horizontal	951.3	mm	
	Vertical	170.8	mm	
	Depth (Dmin)	11.4	mm	Front bezel to Back Bezel
	Depth (Dmax)	28.8	mm	Front Bezel to DB Cover
	Bezel opening	923.3(H) x 142.8(V)	mm	
	Bezel Width	14/14/14/14	mm	U/D/L/R
	Display Area	919.3(H) x 138.85(V)	mm	
Weight	2.7		Kg	

## Front View

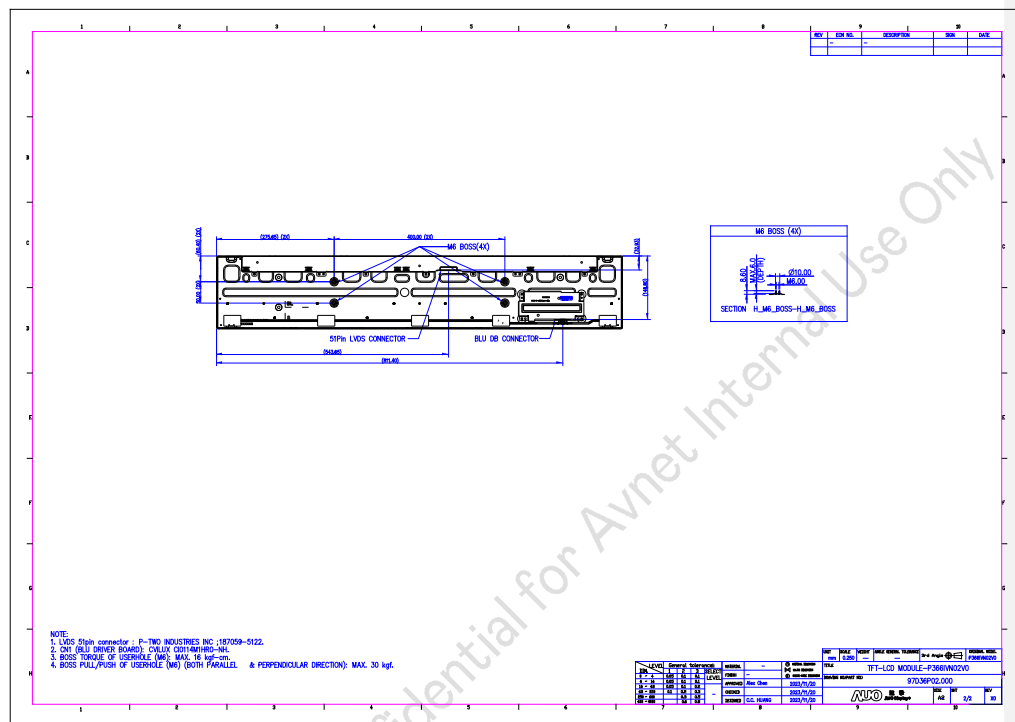


### 已註解 [B21]:

- 1.請 RD 註記平整度規格於圖面
- 2.圖紙 model name 須和產品一致,無須提供 part #
- 3.請 R&D 提供直式圖檔 wmf(圖檔 model name 在右  
上,勿用橫式 wmf 選轉,以免圖型模糊
- 4.注意圖面是否有破線破面
- 5.標明 Driver board pin1 位置



## Back View



### 已註解 [B22]:

- 6.請 RD 註記平整度規格於圖面
- 7.圖紙 model name 須和產品一致,無須提供 part #
8. 請 R&D 提供直式圖檔 wmf(圖檔 model name 在右上,勿用橫式 wmf 選轉,以免圖型模糊)
- 9.注意圖面是否有破線破面
- 10.標明 Driver board pin1 位置

## 8. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60°C, 500hrs
2	Low temperature storage test	3	-25°C, 500hrs
3	High temperature operation test	3	50°C, 500hrs
4	High temperature and High humidity operation (THB)	3	60°C 75%, 500hrs
5	Low temperature operation test	3	-25°C, 500hrs
6	Vibration test (With carton)	1( PKG)	Random wave (1.04Grms 2~200Hz) Duration : X,Y,Z 20min per axes
7	Drop test (With carton)	1( PKG)	Height: 45.7cm Direction: 1 corner 3 edges 6 flats (ASTMD4169-I)

已註解 [B23]: -20~60°C 選用此表

已註解 [B24]: 若整箱重量小於 68Kg, 請參照包裝測試規範

## 9. International Standard

### 9.1 Safety

- (1) UL 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.
- (2) IEC 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.
- (3) EN 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

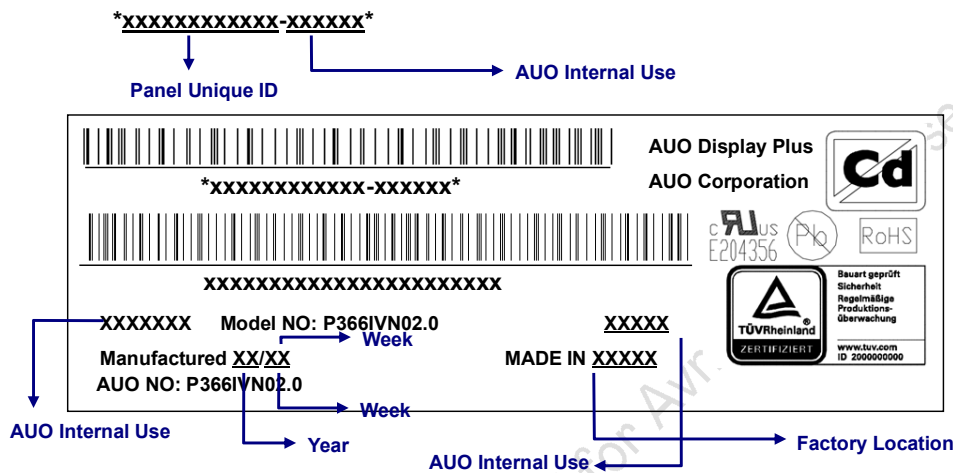
### 9.2 EMC

- (1) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz." American National standards Institute(ANSI), 1992
- (2) C.I.S.P.R "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special committee on Radio Interference.
- (3) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization. (CENELEC), 1998

## 10. Packing

### 10.1 Definition of Label

#### A. Panel Label:



#### Green mark description

- (1) For Pb Free Product, AUO will add for identification.
- (2) For RoHS compatible products, AUO will add for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

#### B. Carton Label:

AUO Display Plus  
MODEL NO : P3661VN02.0  
PART NO : 97D36P02.000  
AUO Corporation  
MODEL NO : P3661VN02.0  
PART NO : 97.36P02.000

QTY: 6

RoHS

CUSTOMER NO: XXXXX-XXXXX-XXXXX

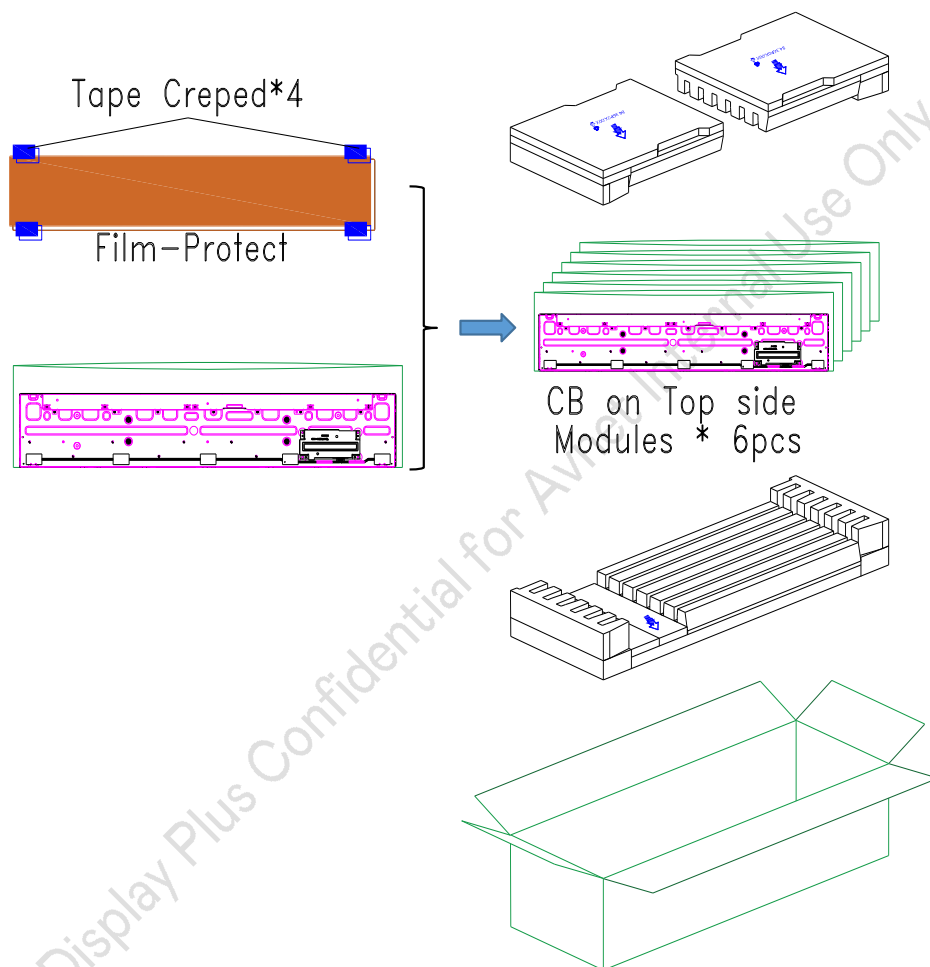
CARTON NO:

Made in XXXXXX

\*XXXXXXXX-XXXXXX\*

已註解 [P25]: 請依實際狀況修改 carton 標籤的數量, 型號, 料號, 料號後兩碼為 XX

## 10.2 Packing Methods

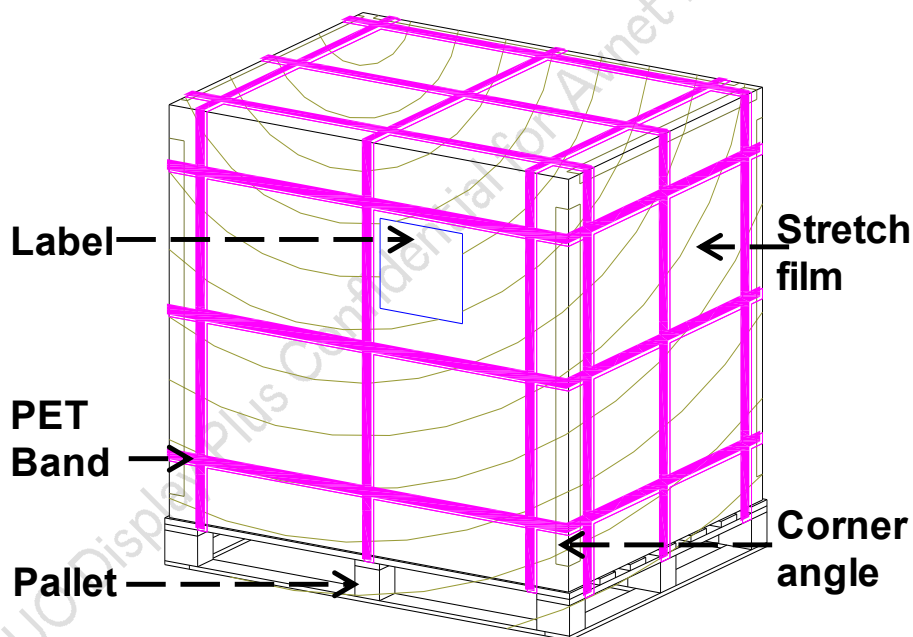


已註解 [B26]: 請向包材 RD 索取該機種包裝規範圖面,  
須註明 Control board 擺放方向

- 1.CB on bottom side
- 2.CB on top side
- 3.CB on middle side

### 10.3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	6pcs/box	1041(L)mm*380 (W)mm*300(H)mm	27	
2	Pallet	1	1150mm*1100mm*132mm(T42)	16	
3	Boxes per Pallet	12 boxes/Pallet (By Air) ; 9Boxes/Pallet (By Sea)			Sea->Double Pallet
4	Panels per Pallet	72 pcs/pallet(By Air) ; 54 pcs/Pallet (By Sea)			Sea->Double Pallet
5	Pallet after packing	1(by Air)	1150 (L)mm*1100(W)mm*1332(H)mm	340 (by Air)	
		1 (by Sea)	1150 (L)mm*1100(W)mm*1032(H)mm	259 (by Sea)	40DC Double Pallet



## 11. Precautions

Please pay attention to the followings when you use this TFT LCD module.

### 11.1. Mounting Precautions

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

### 11.2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage:  
 $V = \pm 200\text{mV}$  (Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may

be important to minimize the interface.

- (7) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

### 11.3. Operating Condition for Public Information Display

The device listed in the product specification is designed and manufactured for PID (Public Information Display) application. To optimize module's lifetime and function, below operating usages are required.

(1) Normal operating condition

- A. Operating temperature: -25~60℃
- B. Operating humidity: 10~90%
- C. Display pattern: dynamic pattern (Real display).

Note) Long-term static display would cause image sticking.

(2) Operation usage to protect against image sticking due to long-term static display.

- A. Suitable operating time: under 24 hours a day
- B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
- C. Periodically change background and character (image) color.
- D. Avoid combination of background and character with large different luminance.

(3) Periodically adopt one of the following actions after long time display.

- A. Running the screen saver (motion picture or black pattern)
- B. Power off the system for a while

(4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

(5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc..., it is strongly recommended to contact ADP for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

已註解 [B27]: DT 機種為 5~90%

### 11.4. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.



### 11.5. Precautions for Strong Light Exposure

- (1) Strong light exposure causes degradation of polarizer and color filter.
- (2) To keep display function well as a digital signage application, especially the component of TFT is very sensitive to sunlight, it is necessary to set up blocking device protecting panel from radiation of ambient environment.

### 11.6. Storage

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
- (3) Storage condition is guaranteed under packing conditions.
- (4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

### 11.7. Handling Precautions for Protection Film

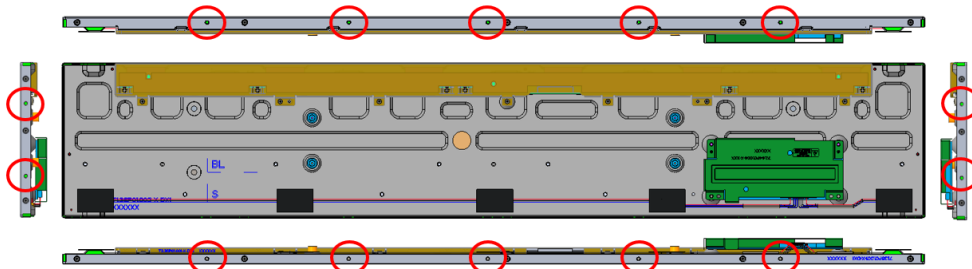
- (1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

### 11.8. Dust Resistance

- (1) AUO module dust tests are conducted with marked holes (see Figure 1) to comply with JIS D0207.
- (2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism.
- (3) ADP's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application.

已註解 [B28]:

Figure 1

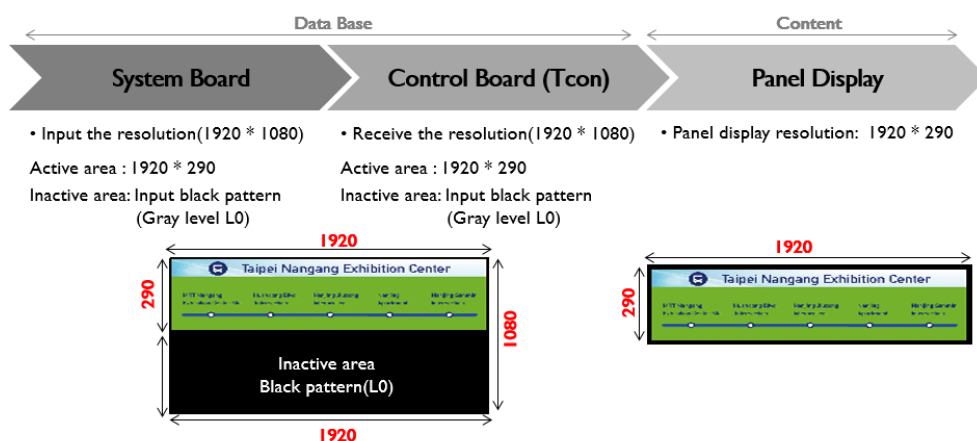


已註解 [eva29]: 請機構 RD 提供圖面

## 12. Appendix: Content Format

- FHD (1920x 1080) / LVDS interface

### FHD (1920 x 1080) / LVDS interface



已註解 [B30]: 非 Tartan 機種請移除此章節