

Model Name: P495IVN02.0

Issue Date: 2025/05/20

(*)Final Specifications
(*)Final Specifications

Customer Signature	Date	AUO Display Plus	Date
Approved By	NE 20250	Approval By PM Director	
Note	isplay P	Reviewed By RD Director Lamy Chen Reviewed By Project Leader	
AUO P For AV		Horis Wang Prepared By PM Kimkuo	



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Record of Revision

Version	Date	Page	Description
0.0	2021/06/18	All	First version release
1.0	2021/12/10	6	Operation / storage condition diagram
1.0	2021/12/10	7	Rx,Ry modify and Viewing Angle typ 85°
1.0	2021/12/10	14	input color data 10bit → 8bit
1.0	2021/12/10	20	BL input current & inrush current & power
1.0	2021/12/10	26/27	Mechanical Front View/ Back View
1.1	2022/05/18	4	Modify second paragraph description of general description part.
1.1	2022/05/18	4-5	New add the spec of sunglasses readability in general information table and Note 3.
1.1	2022/05/18	7	Delete gamma spec.
1.1	2022/05/18	7	Correct the min. and typ. Value of view angle. Vesirg Angle
1.1	2022/05/18	28	Add the reliaiblity item in red color for the upgraded operation temperature. Test Item: V
1.1	2022/05/18	32	Modify the 10.3 Pallet and Shipment Information as below in red.
1.1	2022/05/18	34	Correct operation temp. from 0-50°C to -20-60°C.
1.1	2022/05/18	35	Update the description of 11.8. Dust Resistance. 11.8. <u>Dust Resistance</u> (1) ADP module dust tests are conducted with marked areas (e.g., holes and slits around the front bezel and back cover) jesaled, to comply with JIS D0207 (see Figure 1). (2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism (3) ADP's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application
1.2	2022/05/26	23	Add Note5 PDIM.
1.3	2022/07/15	7	Remove PST note 3
1.4	2023/03/28	30	Label Update
1.5	2023/04/20	28	Update RA condition
1.6	2024/5/9	4	Pixel Arrangement: add BGR
1.7	2025/5/20	4,5	Revise LED MTTF to MTBF:100Khours, and Note 4 description
		28	Add MTBF test items in Chapter 8 Reliability Test Items



1. General Description

This specification applies to the 49.5 inch Color TFT-LCD Module P495IVN02.0. This LCD module has a TFT active matrix type liquid crystal panel 1920x540 pixels, and diagonal size of 49.5 inch. This module supports 1920x540 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

P495IVN02.0 has been designed to apply the 8-bit 2 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important. Special materials applied into this model are:

- 1. Liquid crystal: Advanced wide temperature LC(-40°C-110°C)
- 2. Polarizer: Wide temperature polarizer (95°C)

* General Information

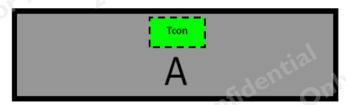
General Information	taro polarizor (ee ey		
Items	Specification	Unit	Note
Active Screen Size	49.5	inch	
Display Area	1209.6(H) x 340.2(V)	mm	
Outline Dimension	1237.4(H) x 368(V) x 25.1(D)	mm	D: front bezel to D/B cover
Driver Element	a-Si TFT active matrix		
Display Colors	8 bit(16.7 million)	Colors	
Number of Pixels	1920 x 540	Pixel	
Pixel Pitch	0.63 (H) x 0.63 (W)	mm	
Pixel Arrangement	RGB&BGR vertical stripe		jal
Display Operation Mode	Normally Black	e ye	anly .
Surface Treatment	Anti-Glare, 3H	U_{II}	Haze = 28%
Rotate Function	Unachievable	10	Note 1
Display Orientation	Portrait/Landscape Enabled	U.o.	Note 2
Sunglasses Readability	Landscape Mode		Note 3
Operating Time	24/7	7	See Chapter 11.3 for details
Frame Rate	60	Hz	See Chapter 5.1 for details
MTBF	100K	hours	See Chapter 8 for details Note 4



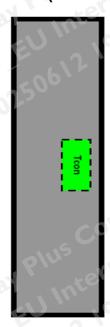
Note 1: Rotate Function refers to LCD display could be able to rotate. This function does not work in this model. Note 2:

- (1) Landscape Mode: The default placement is T-Con Side on the upside and the image is shown upright via viewing from the front.
- (2) Portrait Mode: The default placement is that T-Con side has to be placed on the right side via viewing from the front.





Portrait (Front view)



Note 3:

The image can be seen via polarized sunglasses while this panel is placed in landscape mode.

Display Orientation:



Landscape



Portrait



Polarized Sunglasses

Note 4:

MTBF is a reference index, it is not representative of warranty. Thermal acceleration factor based on Arrhenius model with eV = 0.6 @ Ambient temp 25C/50



2. Absolute Maximum Ratings

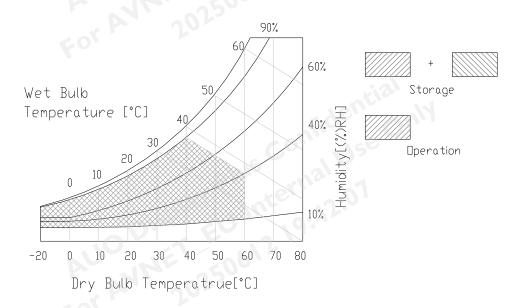
The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	-20	60	[°C]	Note 2
Operating Humidity	НОР	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	

Note 1: Duration:50 msec.

Note 2: Maximum Wet-Bulb should be 39°Cand No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C

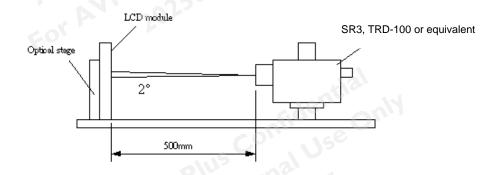




3. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are at an approximate distance 500 mm from the LCD surface at a viewing angle of φ and θ equal to 0° .

Fig.1 presents additional information concerning the measurement equipment and method.



	Devemeter	Cyrophol		Values		l lm:t	Notes
	Parameter	Symbol	Min.	Тур.	Max	Unit	Notes
Contrast	Ratio	CR	3200	4000			1
Surface	Luminance (White)	Lwh	2000	2500		cd/m ²	2
Luminan	ce Variation	δwнitе(9Р)			1.33		3
Respons	e Time (G to G)	Тү	8		16	ms	4
Color Ga	amut	sRGB		72	1/	%	
Color Co	ordinates			dia	$O_{LL_{LL_{1}}}$		
	Red	Rx	, C ₀	0.609			
		R _Y	Inz	0.328			
	Green	Gx	" "FEI	0.341			
		G _Y	T . 0.00	0.568	T 0 00		
	Blue	Bx	Typ0.03	0.166	Тур.+0.03		
		By		0.115			
	White	Wx		0.313			
		W _Y		0.329			
Viewing .	Angle				al		5
	x axis, right(φ=0°)	θ_{r}	85	89		degree	
	x axis, left(φ=180°)	θι	85	89	O''	degree	
	y axis, up(φ=90°)	θ_{u}	85	89		degree	
	y axis, down (φ=270°)	$\theta_{\sf d}$	85	89		degree	



Note:

1. Contrast Ratio (CR) is defined mathematically as:

- 2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. LED current I_F = typical value (without driver board), LED input VDDB =24V, I_{DDB}. = Typical value (with driver board), L_{WH}=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.
- 3. The variation in surface luminance, δWHITE is defined (center of Screen) as: δ_{WHITE(9P)}= Maximum(L_{on1}, L_{on2},...,L_{on9})/ Minimum(L_{on1}, L_{on2},...L_{on9})
- 4. Response time T_{γ} is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured			Target												
Respo	onse Time	0%	25%	50%	75%	100%									
	0% 0% to 25% 25% to 0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%									
				25% to 50%	25% to 75%	25% to 100%									
Start	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%									
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%									
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%										

Ty is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray(bright)" and "any level of gray(dark)".

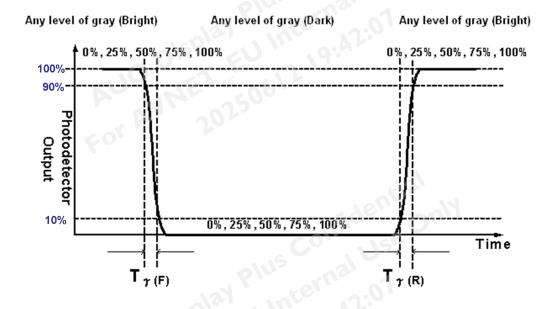
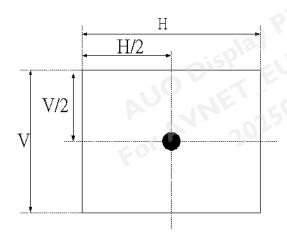
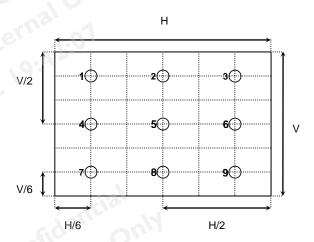




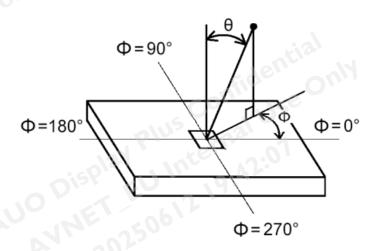
FIG. 2 Luminance





5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG3.

FIG.3 Viewing Angle





4. Interface Specification

4.1 Input power

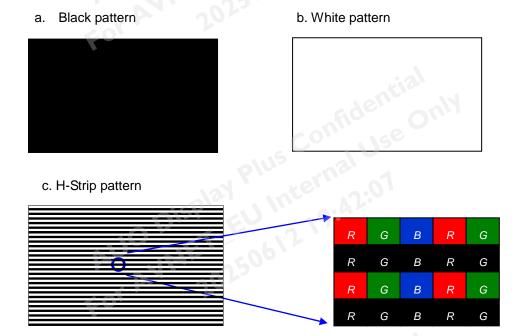
The P495IVN02.0 module requires power inputs which are employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item	0 -1	Symbol	Min.	Тур.	Max	Unit	Note
Power Supply Input Voltage	17/1/20	V_{DD}	10.8	12	13.2	V	1
	Black pattern		-	0.34	0.41	Α	
Power Supply Input Current	White pattern	I _{DD}	-	0.35	0.42	Α	
	H-strip pattern		-	0.41	0.49	Α	2
	Black pattern		750	4.08	4.90	Watt	2
Power Consumption	White pattern	Pc	60	4.20	5.04	Watt	
	H-strip pattern	Co,	, 1)	4.92	5.90	Watt	
Inrush Current	01	I _{RUSH}	9/"		2.86	Α	3

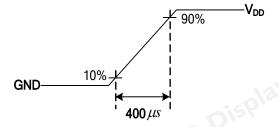
Note1. The ripple voltage should be fewer than 5% of VDD.

Note2. Test Condition:

- (1) $V_{DD} = 12.0V$, (2) $F_{V} = 60Hz$, (3) $F_{C} = 74.25MHz$, (4) $T_{C} = 25 ^{\circ}C$
- (5) Power dissipation check pattern. (Only for power design)



Note3. Measurement condition : Rising time = 400us





4.2 Input Connection

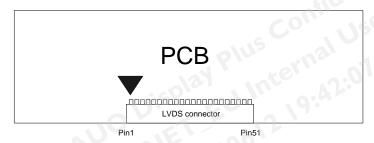
LCD connector:

P-Two 187059-51221-1 / Starconn 115E51-0000RA-M3-R / JAE SJ11346-FI-RTE51SZ-HF

N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. CH1_0- CH1_1- CH1_1+ CH1_1+ CH1_2- CH1_2+	No connection No connection No connection No connection No connection No connection Open/ Low (GND) for NS High (3.3V) for JEIDA No connection No connection No connection Cround LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 12- LVDS Channel 1, Signal 2- LVDS Channel 1, Signal 2-	1&2 2 2 2 2 2 3&4 2 2 2	26 27 28 29 30 31 32 33 34 35 36 37 38 39	N.C. N.C. CH2_0- CH2_0+ CH2_1- CH2_1+ CH2_2- CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3- CH2_3-	No connection No connection LVDS Channel 2, Signal 0- LVDS Channel 2, Signal 0+ LVDS Channel 2, Signal 1- LVDS Channel 2, Signal 1+ LVDS Channel 2, Signal 2- LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3- LVDS Channel 2, Signal 3-	2 2
N.C. N.C. N.C. VDS_SEL N.C. N.C. N.C. GND CH1_0- CH1_1- CH1_1+ CH1_2- CH1_2+	No connection No connection No connection No connection Open/ Low (GND) for NS High (3.3V) for JEIDA No connection No connection No connection Ground LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	2 2 2 2 3&4 2 2	28 29 30 31 32 33 34 35 36 37 38 39	CH2_0- CH2_0+ CH2_1- CH2_1+ CH2_2- CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3-	LVDS Channel 2, Signal 0- LVDS Channel 2, Signal 0+ LVDS Channel 2, Signal 1- LVDS Channel 2, Signal 1+ LVDS Channel 2, Signal 2- LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	2
N.C. N.C. VDS_SEL N.C. N.C. N.C. GND CH1_0- CH1_1- CH1_1+ CH1_2- CH1_2+	No connection No connection No connection Open/ Low (GND) for NS High (3.3V) for JEIDA No connection No connection No connection Ground LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	2 2 2 3&4 2 2	29 30 31 32 33 34 35 36 37 38 39	CH2_0+ CH2_1- CH2_1+ CH2_2- CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3-	LVDS Channel 2, Signal 0+ LVDS Channel 2, Signal 1- LVDS Channel 2, Signal 1+ LVDS Channel 2, Signal 2- LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Clock +	
N.C. N.C. VDS_SEL N.C. N.C. GND CH1_0- CH1_1- CH1_1+ CH1_2- CH1_2+	No connection No connection Open/ Low (GND) for NS High (3.3V) for JEIDA No connection No connection Ground LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1-	2 2 3&4 2 2	30 31 32 33 34 35 36 37 38	CH2_1- CH2_1+ CH2_2- CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3-	LVDS Channel 2, Signal 1- LVDS Channel 2, Signal 1+ LVDS Channel 2, Signal 2- LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Clock +	
N.C. VDS_SEL N.C. N.C. N.C. GND CH1_0- CH1_1- CH1_1- CH1_1+ CH1_2- CH1_2+	No connection Open/ Low (GND) for NS High (3.3V) for JEIDA No connection No connection Ground LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1-	2 3&4 2 2	31 32 33 34 35 36 37 38 39	CH2_1+ CH2_2- CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3-	LVDS Channel 2, Signal 1+ LVDS Channel 2, Signal 2- LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	
N.C. N.C. N.C. GND CH1_0- CH1_1- CH1_1+ CH1_2- CH1_2+	Open/ Low (GND) for NS High (3.3V) for JEIDA No connection No connection Oround LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 1-	3&4 2 2	32 33 34 35 36 37 38 39	CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3-	LVDS Channel 2, Signal 2- LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	
N.C. N.C. GND CH1_0- CH1_1- CH1_1+ CH1_1+ CH1_2- CH1_2+	High (3.3V) for JEIDA No connection No connection Ground LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1-	2	33 34 35 36 37 38 39	CH2_2+ GND CH2_CLK- CH2_CLK+ GND CH2_3-	LVDS Channel 2, Signal 2+ Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	
N.C. N.C. GND CH1_0- CH1_1- CH1_1- CH1_1+ CH1_2- CH1_2+	No connection No connection Ground LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	2	34 35 36 37 38 39	GND CH2_CLK- CH2_CLK+ GND CH2_3-	Ground LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	
N.C. GND CH1_0- CH1_1- CH1_1- CH1_1+ CH1_2- CH1_2+	No connection Ground LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	-	35 36 37 38 39	CH2_CLK+ CH2_CLK+ GND CH2_3-	LVDS Channel 2, Clock - LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	
GND CH1_0- CH1_0+ CH1_1- CH1_1+ CH1_2- CH1_2+	Ground LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	2	36 37 38 39	CH2_CLK+ GND CH2_3-	LVDS Channel 2, Clock + Ground LVDS Channel 2, Signal 3-	
CH1_0- CH1_0+ CH1_1- CH1_1+ CH1_2- CH1_2+	LVDS Channel 1, Signal 0- LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	10,	37 38 39	GND CH2_3-	Ground LVDS Channel 2, Signal 3-	
CH1_0+ CH1_1- CH1_1+ CH1_2- CH1_2+	LVDS Channel 1, Signal 0+ LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	613	38 39	CH2_3-	LVDS Channel 2, Signal 3-	
CH1_1- CH1_1+ CH1_2- CH1_2+	LVDS Channel 1, Signal 1- LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-	6/1	39			
CH1_1+ CH1_2- CH1_2+	LVDS Channel 1, Signal 1+ LVDS Channel 1, Signal 2-			CH2_3+	LVDS Channel 2. Signal 3+	
CH1_2- CH1_2+	LVDS Channel 1, Signal 2-		40		, , , ,	1
CH1_2+			40	N.C.	No connection	2
	LVDC Observal 4. Observal 0.	1	41	N.C.	No connection	2
	LVDS Channel 1, Signal 2+		42	N.C.	No connection	2
GND	Ground		43	N.C.	No connection	2
H1_CLK-	LVDS Channel 1, Clock -		44	GND	Ground	
H1_CLK+	LVDS Channel 1, Clock +	115	45	GND	Ground	
GND	Ground	-	46	GND	Ground	
CH1_3-	LVDS Channel 1, Signal 3-	110,	47	N.C.	No connection	2
CH1_3+	LVDS Channel 1, Signal 3+		48	V_{DD}	Power Supply Input Voltage	
N.C.	No connection	2	49	V_{DD}	Power Supply Input Voltage	
N.C.	No connection	2	50	V_{DD}	Power Supply Input Voltage	
	FOL	•	51	V_{DD}	Power Supply Input Voltage	
C	GND CH1_3- CH1_3+ N.C. N.C.	GND Ground CH1_3- LVDS Channel 1, Signal 3- CH1_3+ LVDS Channel 1, Signal 3+ N.C. No connection N.C. No connection	GND Ground CH1_3- LVDS Channel 1, Signal 3- CH1_3+ LVDS Channel 1, Signal 3+ N.C. No connection 2 N.C. No connection 2	GND Ground 46 CH1_3- LVDS Channel 1, Signal 3- 47 CH1_3+ LVDS Channel 1, Signal 3+ 48 N.C. No connection 2 49 N.C. No connection 2 50	GND Ground 46 GND CH1_3- LVDS Channel 1, Signal 3- 47 N.C. CH1_3+ LVDS Channel 1, Signal 3+ 48 V _{DD} N.C. No connection 2 49 V _{DD} N.C. No connection 2 50 V _{DD} 51 V _{DD}	GND Ground 46 GND Ground CH1_3- LVDS Channel 1, Signal 3- 47 N.C. No connection CH1_3+ LVDS Channel 1, Signal 3+ 48 V _{DD} Power Supply Input Voltage N.C. No connection 2 49 V _{DD} Power Supply Input Voltage N.C. No connection 2 50 V _{DD} Power Supply Input Voltage



Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

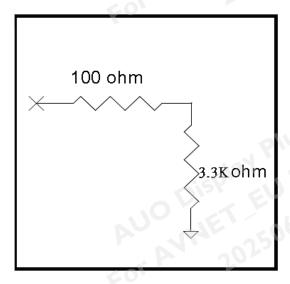
Note3. Input control signal threshold voltage definition

Item	Symbol	Min.	Тур.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	- 2	3.6	>
Input Low Threshold Voltage	VIL	0		0.6	٧

Note4. LVDS data format selection

LVDS_SEL	Mode
L or OPEN	NS
Н	Jeida

Input equivalent impedance of LVDE_SEL pin



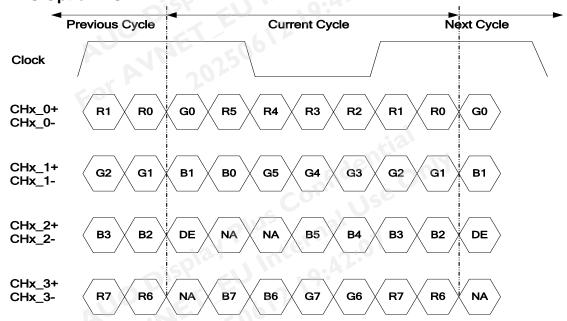


4.3 Input Data Format

4.3.1 LVDS color data mapping

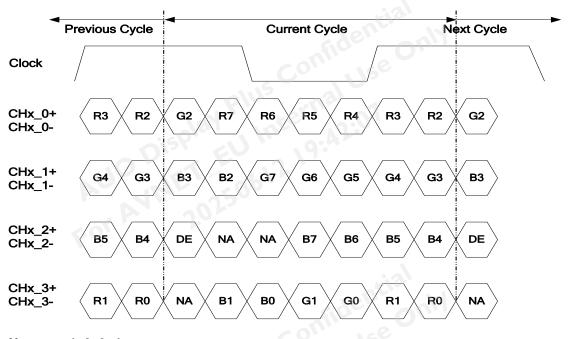
LVDS Option for 8bit

■ LVDS Option NS



Note: x = 1, 2, 3, 4...

■ LVDS Option JEIDA



Note: x = 1, 2, 3, 4...



4.3.2 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

DATA REFERENCE COLOR

·	Color																								
		RED				25				(GRI	EEN							BLUE						
			В	D.F.	D.4	D 0	DO	LS		MS		05	0.4	00	00	LS		MS		D.E.			DO	LS	
	<u> </u>	R7	R6			R3		R1			G6				G2								B2		BO
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
F	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
<u>.</u> .	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
-	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
F	Magenta	1	1	1	1	1	1	1	1	0	0	0	0 1	0	0	0	0	1	1	1	1	1	1	1	1
-	Yellow	1	1	1	1	1	1	1		1	1			1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
F	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	 DED(054)								^					^							_	_	^		^
F	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
F	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(001)	0	0	0	0	0	0	0	0	U	0	0	U	U	0	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	.1	1	1	1	0	0	0	0	0	0	0	0	0
F	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	GREEN(255) BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
В	BLUE(UUT)	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	ı
-	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
F	BLUE(255)																		1	1	1	1	1	1	1
	DLOL(233)	U	U	U	U	U	U	U	U	U	U	U	U		U	U	U	, ,	<u>'</u>		<u> </u>	<u>'</u>	'	'	
			y P U i				1		ال																
© Copyr	right AUO Dis	spla	y P	lus	Co	rpo	rati	on	202	25 A	II R	igh	ts I	Res	erv	ed.					Ρ	age	14	/ 30	3



5. Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Input Timing

5.1.1. Timing table

Timing Table (DE only Mode)

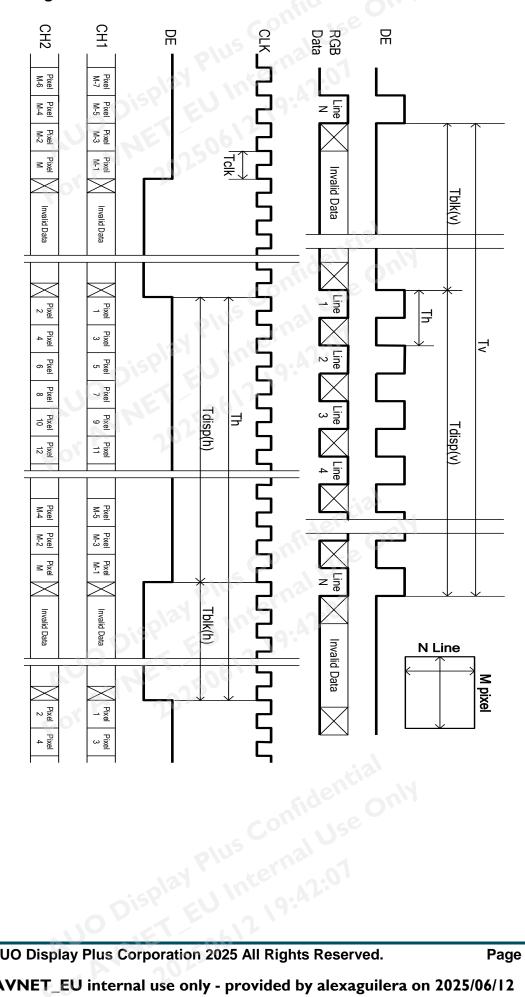
Signal	Item	Symbol	Min.	Тур.	Max	Unit
	Period	Tv	1120	1125	1480	Th
Vertical Section	Active	Tdisp (v)	16UCI	1080		
	Blanking	Tblk (v)	40	45	400	Th
	Period	Th	1030	1100	1325	Tclk
Horizontal Section	Active	Tdisp (h)	3.1			
	Blanking	Tblk (h)	70	140	365	Tclk
Clock	Frequency	Fclk=1/Tclk	53	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz

Notes:

- (1) Display position is specific by the rise of DE signal only. Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.
- (2) Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.
- (3) If a period of DE "High" is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.
- (4) The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.



5.1.2. Signal Timing Waveform

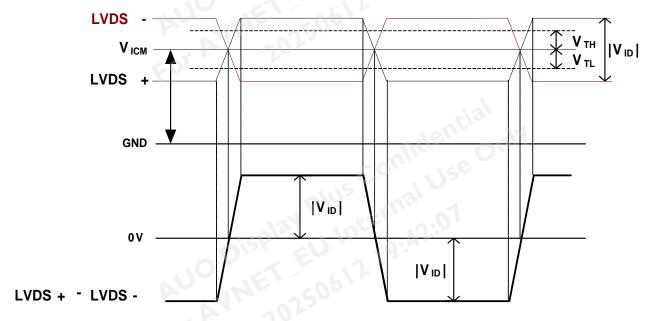




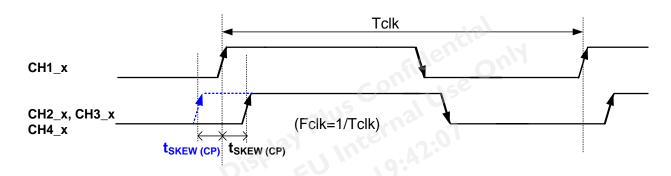
5.2 Input interface characteristics

	Parameter		103	Value		Unit	Note
	raiametei	Symbol	Min.	Тур.	Max	Offic	Note
	Input Differential Voltage	V _{ID}	200	400	600	mV _{DC}	1
	Differential Input High Threshold Voltage	V _{тн}	+100		+300	mV _{DC}	1
	Differential Input Low Threshold Voltage	V _{TL}	-300		-100	mV _{DC}	1
	Input Common Mode Voltage	VICM	1.1	1.25	1.4	V _{DC}	1
LVDS	Input Channel Pair Skew Margin	tskew (CP)	-500	-	+500	ps	2
Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	-inly	Fclk +3%	MHz	3
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	1	200	KHz	3
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	-0.4 -0.5		0.4 0.5	ns	8

Note1. VICM = 1.25V

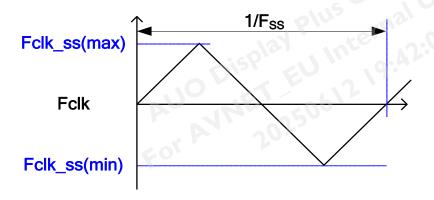


Note2. Input Channel Pair Skew Margin



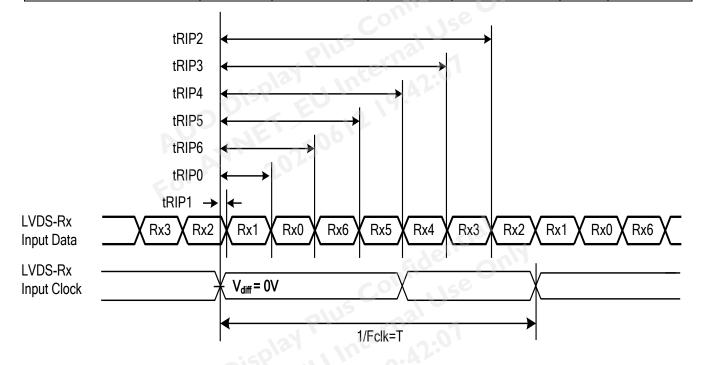


Note3. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



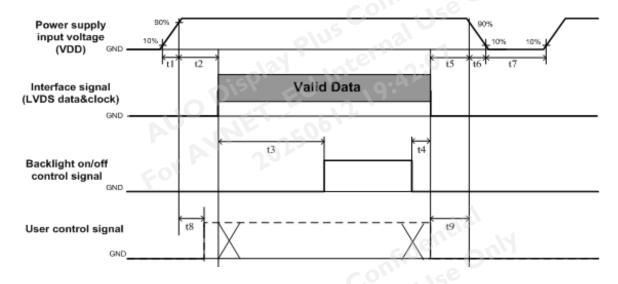
Note4. Receiver Data Input Margin

Doromotor	Symbol	Rating		Unit	Note	
Parameter	Symbol	Min	Туре	Туре Мах		Note
Input Clock Frequency	Fclk	Fclk (min)	17:0	Fclk (max)	MHz	T=1/Fclk
Input Data Position0	tRIP1	- tRMG	0	tRMG	ns	
Input Data Position1	tRIP0	T/7- tRMG	T/7	T/7+ tRMG	ns	
Input Data Position2	tRIP6	2T/7- tRMG	2T/7	2T/7+ tRMG	ns	
Input Data Position3	tRIP5	3T/7- tRMG	3T/7	3T/7+ tRMG	ns	
Input Data Position4	tRIP4	4T/7- tRMG	4T/7	4T/7+ tRMG	ns	
Input Data Position5	tRIP3	5T/7- tRMG	5T/7	5T/7+ tRMG	ns	
Input Data Position6	tRIP2	6T/7- tRMG	6T/7	6T/7+ tRMG	ns	





Power Sequence for LCD 5.3



B	0	l lada		
Parameter	Min.	Type.	Max.	Unit
t1	0.4	/2:	30	ms
t2	40	612		ms
t3	640			ms
t4	0*1			ms
t5	0			ms
t6			*2	ms
t7	1000		00	ms
t8	20 ^{*3}	Cor. 'Ne	50	ms
t9	0	102 11/31		ms

Note:

- (1) t4=0 : concern for residual pattern before BLU turn off.
- (2) t6: voltage of VDD must decay smoothly after power-off. (Customer system decide this value)
- (3) When User control signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.



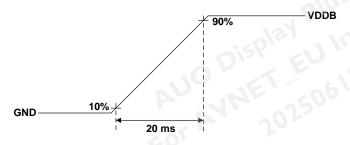
6. Backlight Specification

6.1 Electrical specification

	Item	S	ymbol	Condition	Min	Тур	Max	Unit	Note
1	Power Supply Input Voltage	V	DDB	12-	22.8	24	25.2	V	-
2	Power Supply Input Current	7	I _{DDB}	VDDB=24V		4.47	5.36	А	1
3	Power Consumption		P _{DDB}	VDDB=24V		107.3	135.1	Watt	1
4	Inrush Current	1	RUSH	VDDB=24V	la S		16.32	Α	2
5	Control signal voltage	V	Hi	VDDB-24V	2	-	5.5	V	-
3	Control signal voltage	V _{Signal}	Low	VDDB=24V -	050	-	0.8	V	3
6	Control signal current	ı	Signal	VDDB=24V	- 1	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_	EPWM	VDDB=24V	0	-	100	%	4
8	External PWM Frequency	F_	EPWM	VDDB=24V	120	-	960	Hz	4
	DET status signal		HI	VDDD 24V	Оре	en Colle	ctor	V	5
9	DET status signal	DET	Lo	VDDB=24V	0	-	0.8	V	5
10	Input Impedance		Rin	VDDB=24V	300			Kohm	-
11	LED MTTF	LEC	_MTTF	-	50,000	- 1	1 -	Hr	6, 7

Note 1: Dimming ratio= 100%, (Ta=25±5°C, Turn on for 45minutes)

Note 2: MAX input current while DB turn on, measurement condition VDDB rising time=20ms(VDDB: 10%~90%)



Note 3: When BLU off (VDDB = 24V, VBLON = 0V), IDDB (max) = 0.1A.

Note 4: Less than 5% dimming control is functional well and no backlight shutdown happened.

Note 5: Normal: 0~0.8V; Abnormal: Open collector.

Note 6: The LED MTTF is defined as the time which luminance of LED is 50% compared to its original value.

[Operating condition: Continuous operating at $Ta = 25\pm2^{\circ}C$, for single LED only]

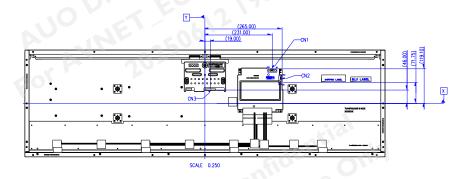
Note 7: MTTF is a reference index, it is not representative of warranty.



6.2 Input Pin Assignment

The P495IVN02.0 module requires 1 power input (14-pin).

CN1 & CN2 (BLU Driver Board) CN3 (TCON Board)



LED DB connector (CN1): No connection (for AUO internal use only)

Pin	Symbol	Description	Not
1	NC	No connection	4
2	NC	No connection	4
3	NC	No connection	4
4	NC	No connection	4
5	NC	No connection	4
6	NC	No connection	4
7	NC	No connection	4
8	NC	No connection	4
9	NC	No connection	4
10	NC	No connection	4
11	NC	No connection	4
12	NC	No connection	4
13	NC	No connection	4
14	NC	No connection	4
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-			=



LED DB connector (CN2): CI0114M1HRL-NH(CviLux) or equivalent

Pin	Symbol	Description	Note
1	VDDB	Power Supply Input Voltage	
2	VDDB	Power Supply Input Voltage	
3	VDDB	Power Supply Input Voltage	
4	VDDB	Power Supply Input Voltage	
5	VDDB	Power Supply Input Voltage	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	DET	BLU status detection:	1
12	VBLON	BLU On-Off control:	2,3
13	NC	NC	4
14	PDIM	External PWM	2,5

Note1. D	ET status		_					
	DET	BLU status						
	0 ~ 0.8V	Normal						
	Open collector	Abnormal						
Recomm	end pull high R > 10	OK ohm, pull high	h voltage	VDD =	3.3V			
Note2. ir	put control signal	threshold volta	age defi	nition	19:4			•
	Item		Symbol	Min.	Тур.	Max.	Unit	
					·		I -	i

Item	Symbol	Min.	Тур.	Max.	Unit
Input High Threshold Voltage	VIH	2	-	5.5	V
Input Low Threshold Voltage	VIL	0	-	8.0	V

Note3. VBLON

Mode selection

VBLON	Note
H or OPEN	BL On
L	BL Off

Note4. Please leave this pin unoccupied. It cannot be connected by any signal (Low/GND/High).



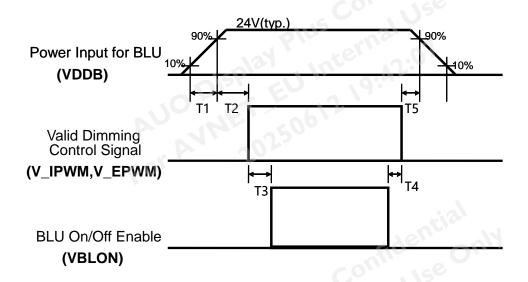
Note5. PDIM

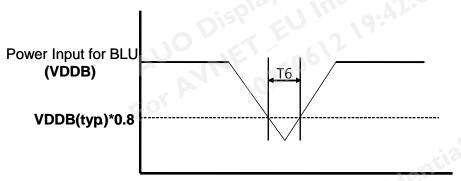


Suggest Dimming PWM signal synchronize and frequency multiplication with cell frame rate



6.3 Power Sequence for Backlight





Dip condition

Parameter	Min	Тур	Max	Units
T1	20	1) 11-	A.L.	ms
T2	250	12	-	ms
Т3	200	600		ms
T4	0	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms ^{*1}

Note1. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.



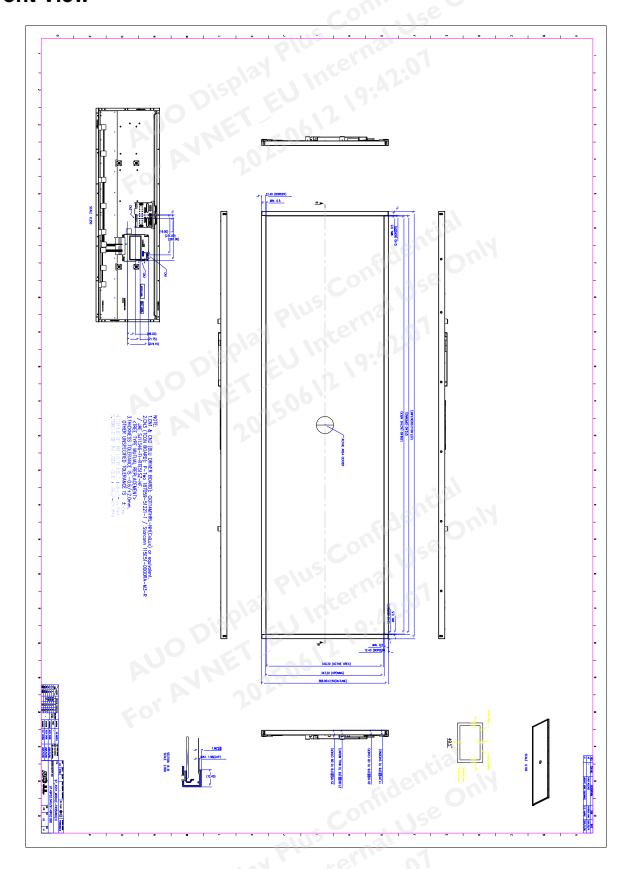
7. Mechanical Characteristics

The contents provide general mechanical characteristics for the model P495IVN02.0. In addition the figures in the next page are detailed mechanical drawing of the LCD.

	Item	Dimension	Unit	Note
	Horizontal	1237.4	mm	
	Vertical	368	mm	
	Depth (Dmin)	10.7	mm	Front bezel to rear
Outline Dimension	Depth (Dmax)	25.1	mm	Front Bezel to DB Cover
	Bezel opening	1212.6(H) x 343.2(V)	mm	
	Bezel Width	12.4/12.4/12.4	mm	U/D/L/R
	Display Area	1209.6(H) x 340.2(V)	mm	
Weight	FOR	6.4	Kg	
		Plus Confident		

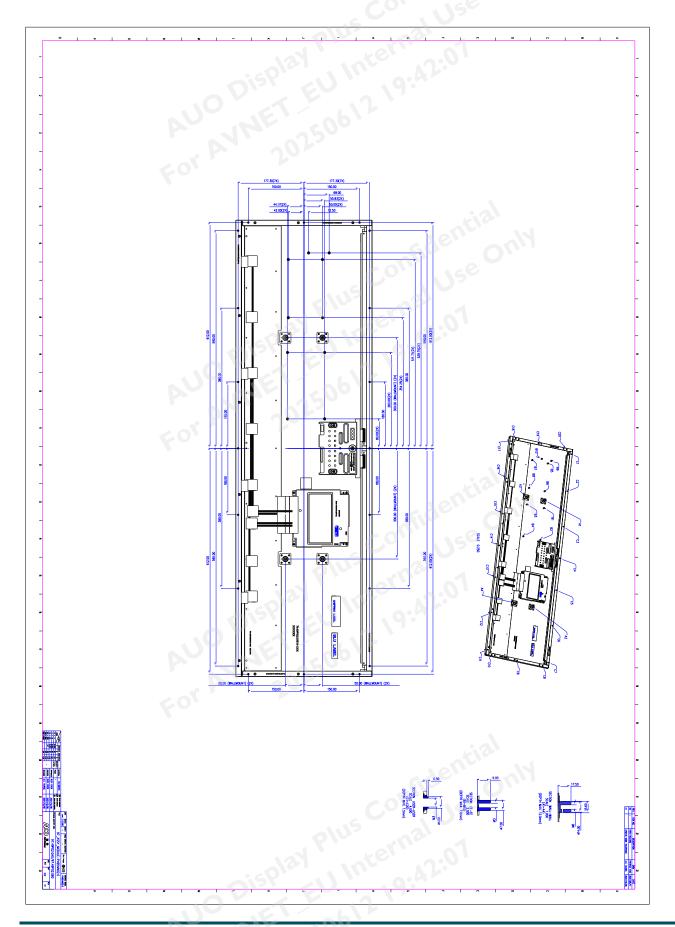


Front View





Back View





8. Reliability Test Items

Test Item	Q'ty	Condition		
High temperature storage test	3	60°Ç 500hrs		
Low temperature storage test	3	-20°C, 500hrs		
High temperature operation test	3	60°C, 500hrs		
Low temperature operation test	3	-20°C, 500hrs		
High temperature and High humidity operation (THB)	3	60°C, 75%, 500hrs		
Vibration test (With carton)	1(PKG)	Random wave (1.04Grms 2~200Hz) Duration: X,Y,Z 20min per axes		
Drop test (With carton)		Height: 45.7 cm Direction: 1-corner \ 3-edges \ 6-flats (ASTMD4169-I)		
Vibration		Time: 5hr(each Axis) Total time: 15hrs Orientation: a) Vertical: 4.25m/s² b) Transverse:2.09m/s² c) Longitudinal: 2.83m/s²		
MTBF	12	50°C/80%, 1300hrs, 90% confidence level		
MTBF AUG DISPIR				



9. International Standard

9.1 Safety

- (1) UL 62368-1: Audio/video, information and communication technology equipment Part 1: Safety requirements
- (2) IEC 62368-1: Audio/video, information and communication technology equipment -Part 1: Safety requirements
- (3) EN 62368-1: Audio/video, information and communication technology equipment -Part 1: Safety requirements

9.2 EMC

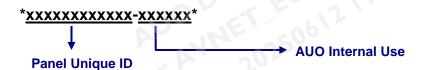
- (1) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. "American National standards Institute(ANSI), 1992
- (2) C.I.S.P.R "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special committee on Radio Interference.
- (3) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization. (CENELEC), 1998

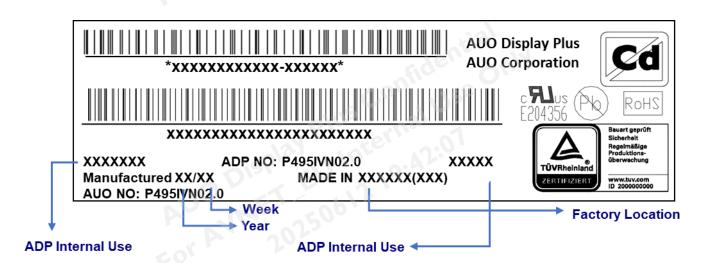


10. Packing

10.1 Definition of Label

A. Panel Label:





Green mark description

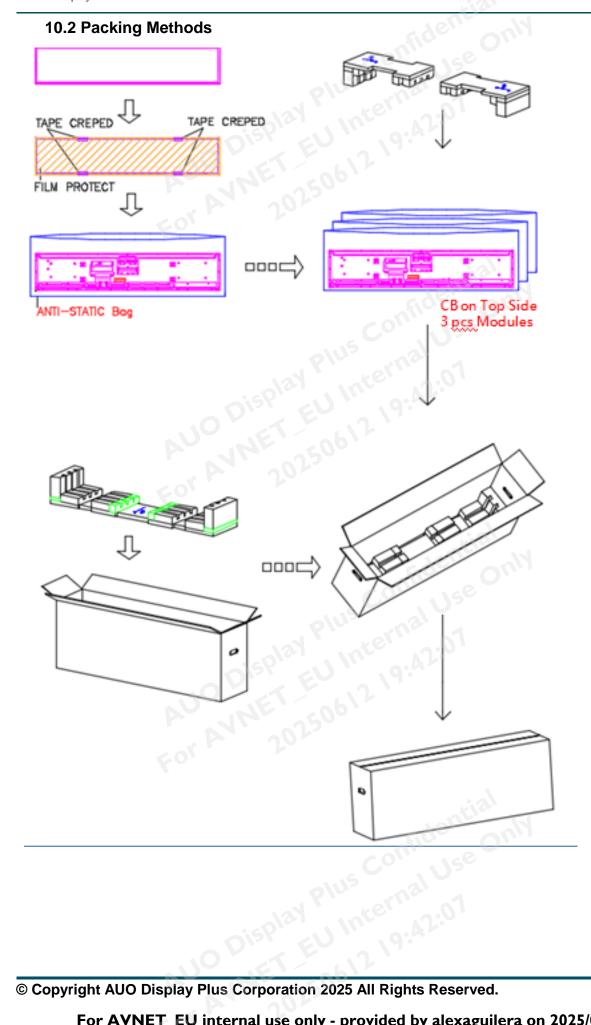
- (1) For Pb Free Product, AUO will add Pb for identification.
- (2) For RoHs compatible products, AUO will add RoHS for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

B. Carton Label:



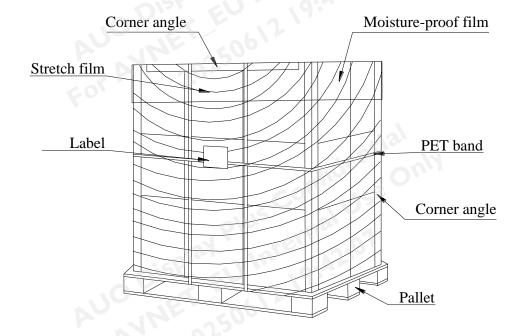






10.3 Pallet and Shipment Information

	Item		Dooking Domork		
	item	Qty.	Qty. Dimension W		Packing Remark
1	Packing BOX	3pcs/box	1350*310*502	25	Box =2.5 kg
					Cushion=1.5 kg
2	Pallet	1	1360*940*138	20	Pallet
3	Boxes per Pallet	6 (3*2)boxes/Pa			
4	Panels per Pallet	18 pcs/pa			
5	Pallet after packing	1	1360*940*1644	245	
		1 pallet (by Sea)	1360*940*1644	245	





11. Precautions

Please pay attention to the followings when you use this TFT LCD module.

11.1. Mounting Precautions

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

11.2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic



interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

(7) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

11.3. Operating Condition for Public Information Display

The device listed in the product specification is designed and manufactured for PID (Public Information Display) application. To optimize module's lifetime and function, below operating usages are required.

- (1) Normal operating condition
 - A. Operating temperature: -20~60°C
 - B. Operating humidity: 10~90%
 - C. Display pattern: dynamic pattern (Real display).Note) Long-term static display would cause image sticking.
- (2) Operation usage to protect against image sticking due to long-term static display.
 - A. Suitable operating time: under 24 hours a day
 - B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
 - C. Periodically change background and character (image) color.
 - D. Avoid combination of background and character with large different luminance.
- (3) Periodically adopt one of the following actions after long time display.
 - A. Running the screen saver (motion picture or black pattern)
 - B. Power off the system for a while
- (4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.
- (5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc..., it is strongly recommended to contact ADP for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

11.4. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.



11.5. Precautions for Strong Light Exposure

- (1) Strong light exposure causes degradation of polarizer and color filter.
- (2) To keep display function well as a digital signage application, especially the component of TFT is very sensitive to sunlight, it is necessary to set up blocking device protecting panel from radiation of ambient environment.

11.6. <u>Storage</u>

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°Cand 35°Cat normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
- (3) Storage condition is guaranteed under packing conditions.
- (4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

11.7. Handling Precautions for Protection Film

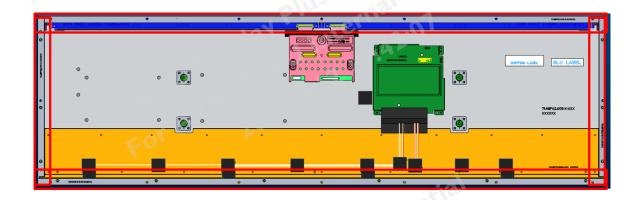
- (1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

11.8. Dust Resistance

- (1) ADP module dust tests are conducted with marked areas (e.g., holes and slits around the front bezel and back cover) sealed, to comply with JIS D0207 (see Figure 1).
- (2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism.
- (3) ADP's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application.



Figure 1 (red mark)



12. Appendix: Content Format

FHD (1920 x 1080) / LVDS interface

