



UltraZed-EV SOM

Revision 1

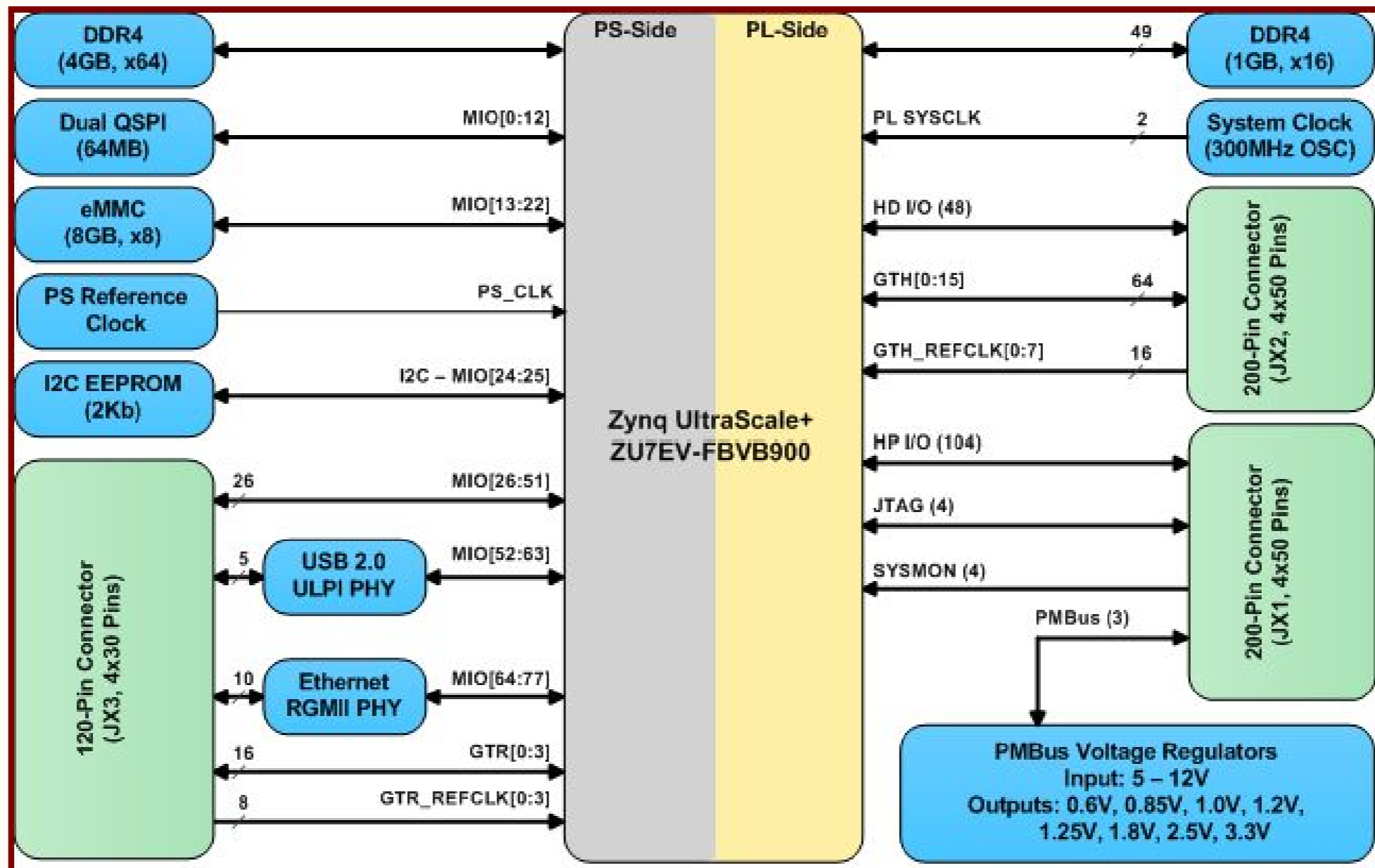
UltraZed-EV SOM	
Avnet Engineering Services	
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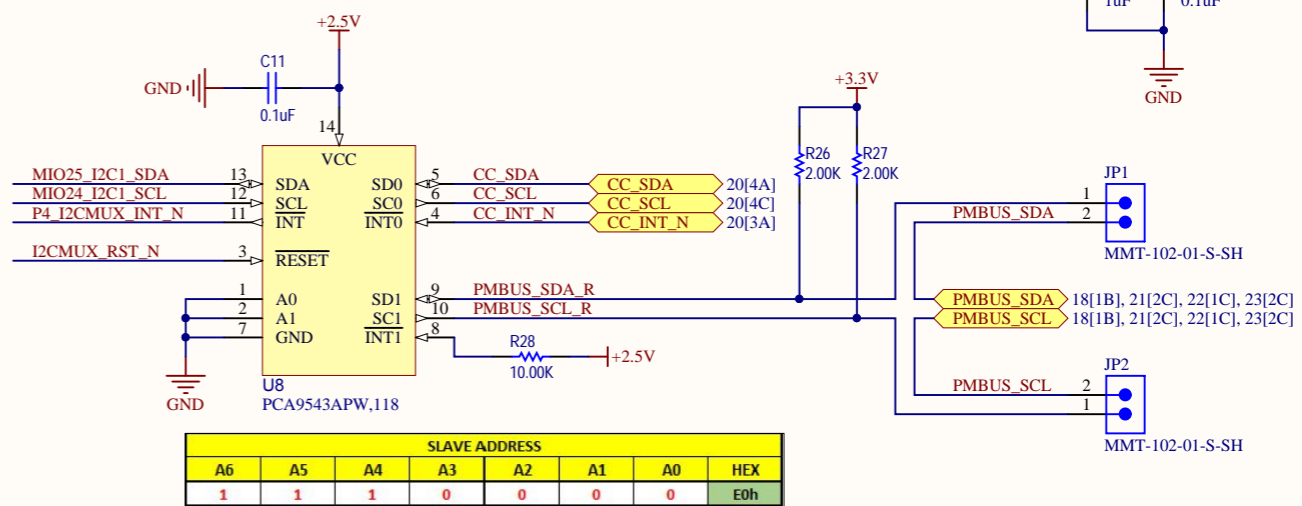
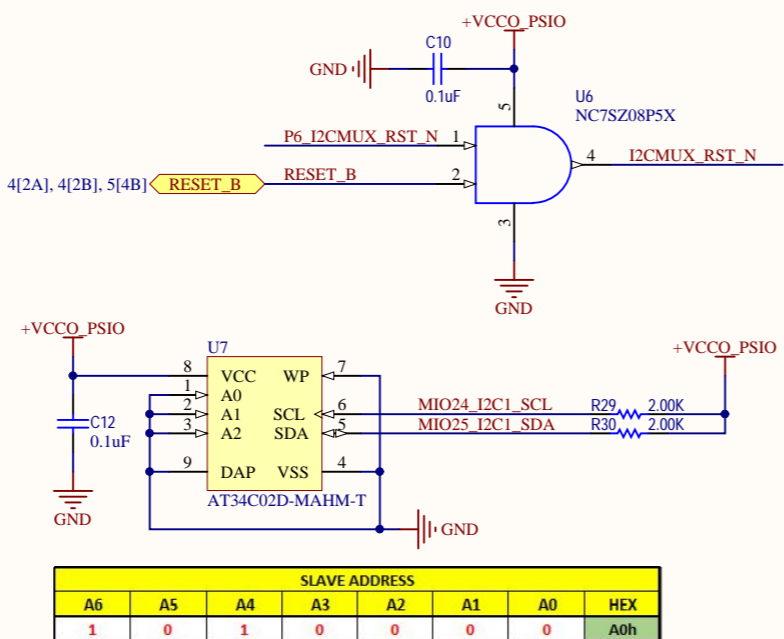
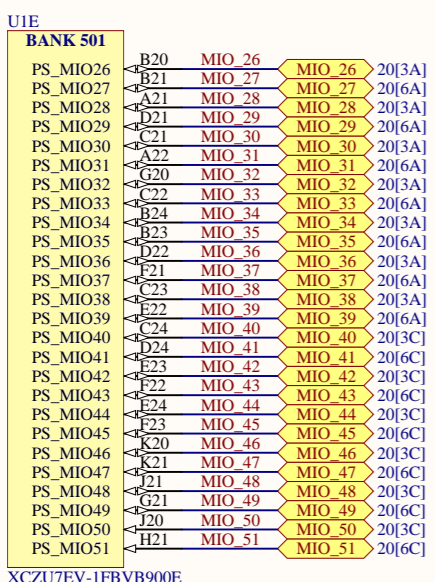
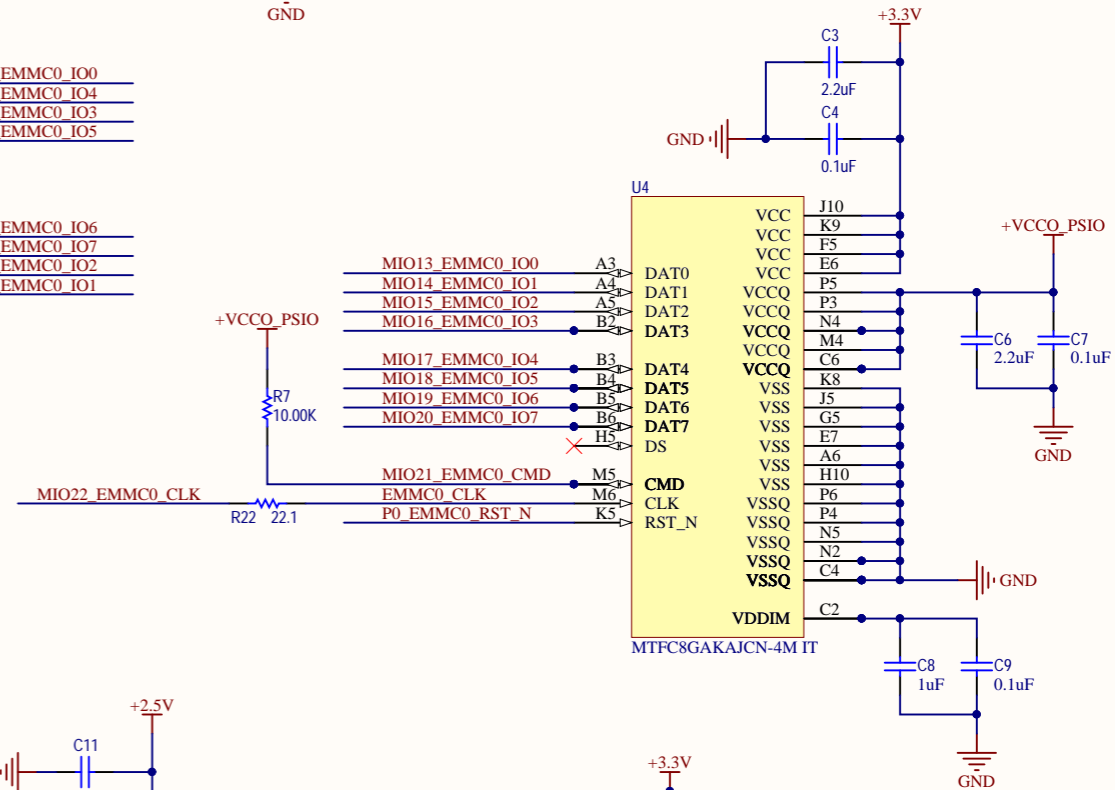
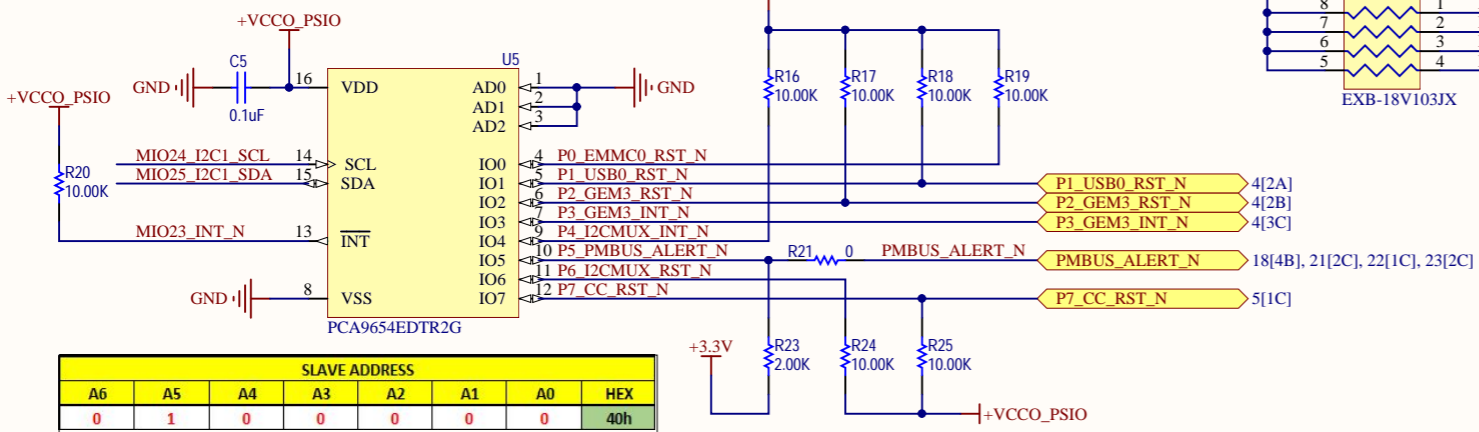
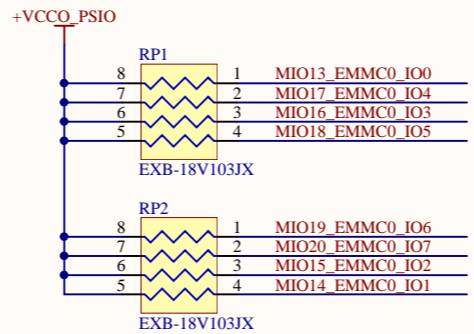
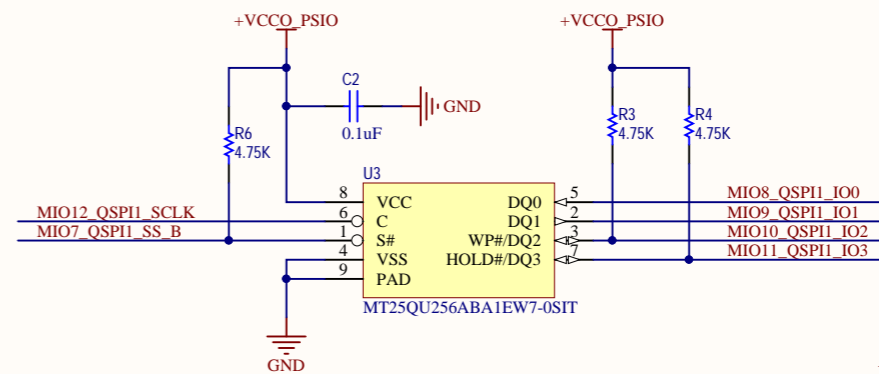
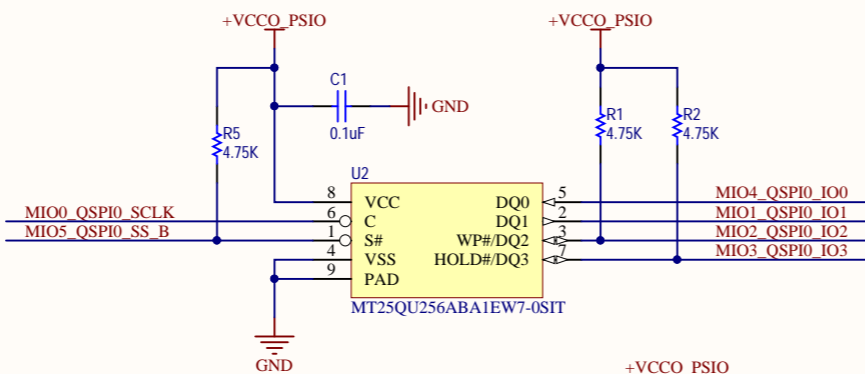
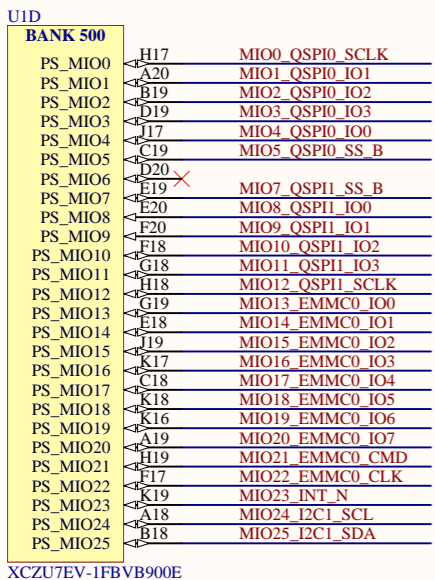
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AVNET Avnet Engineering Services			
Project Name:	UltraZed-EV SOM	PCB Rev:	BOM: Variant:
		1	01 03
Doc Num:	SCH-US2SOM	Date:	Time:
		2/1/2018	4:00:19 PM
Sheet Title:	01 - Avnet Lead Sheet.SchDoc	Size:	Sheet:
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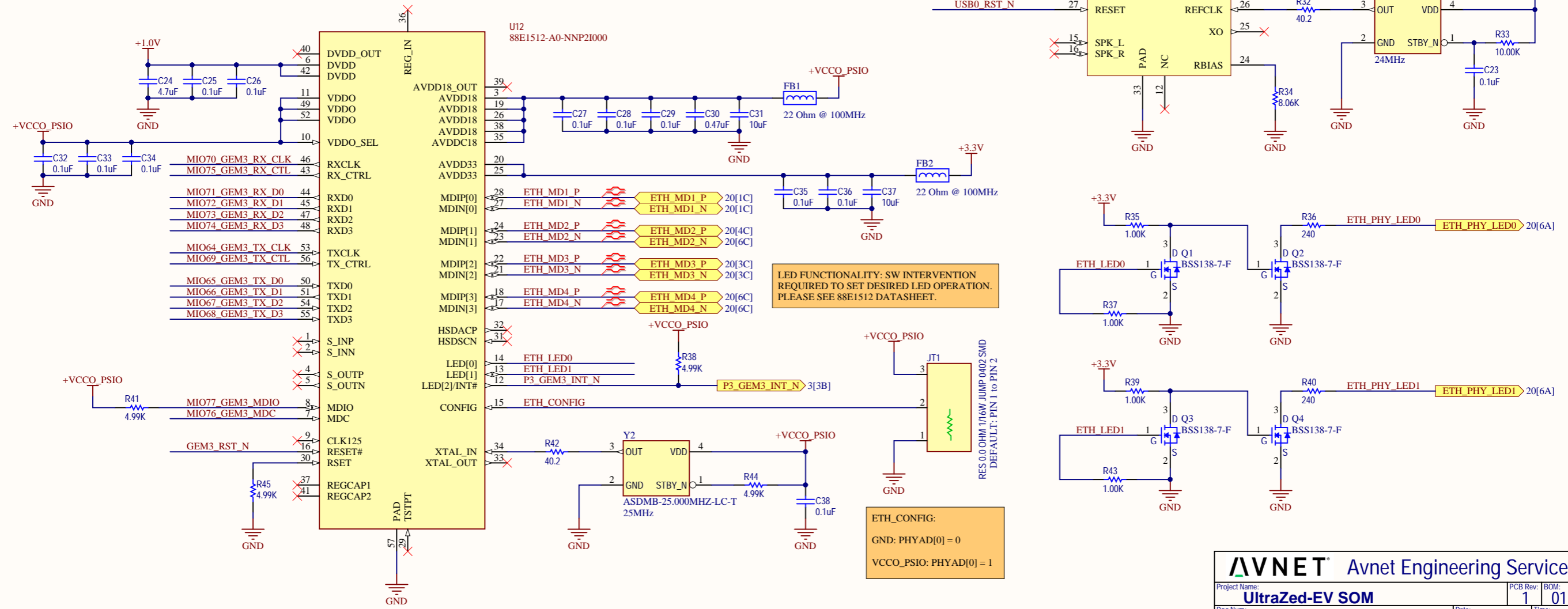
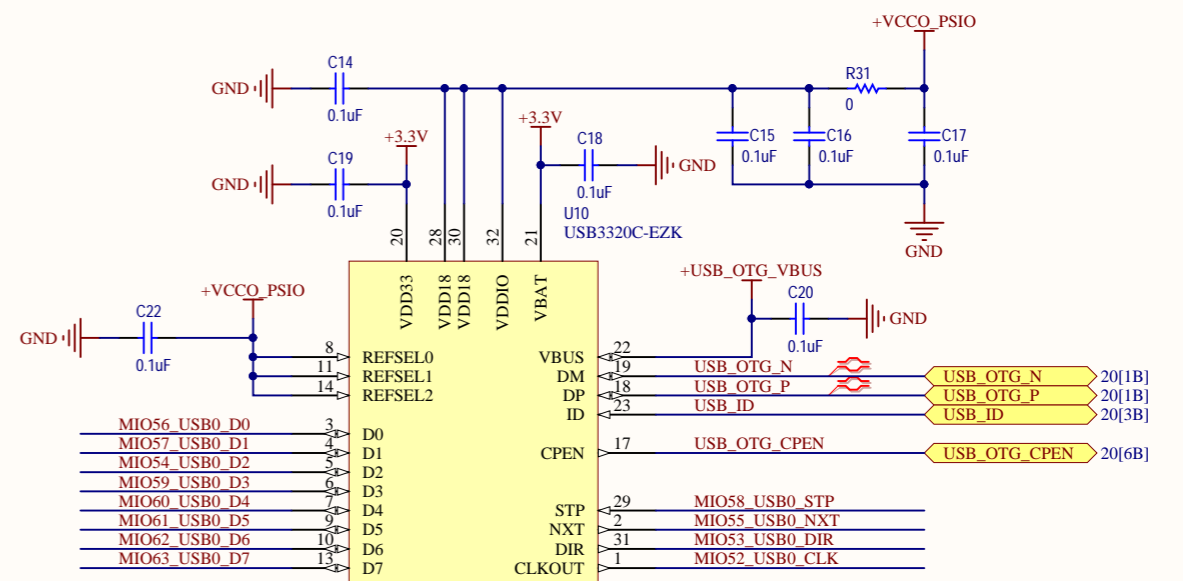
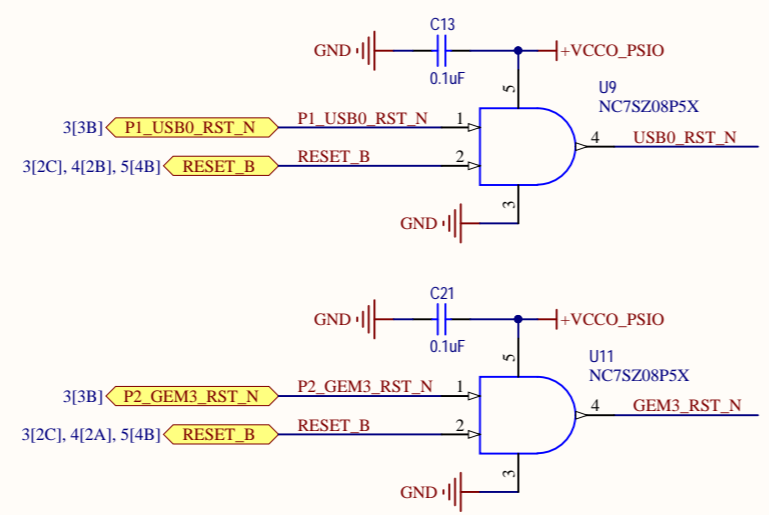




UIF

BANK 502	
PS_MIO52	A24 MIO52 USB0_CLK
PS_MIO53	B25 MIO53 USB0_DIR
PS_MIO54	A23 MIO54 USB0_D2
PS_MIO55	B26 MIO55 USB0_NXT
PS_MIO56	A25 MIO56 USB0_D0
PS_MIO57	A26 MIO57 USB0_D1
PS_MIO58	A28 MIO58 USB0_STP
PS_MIO59	A27 MIO59 USB0_D3
PS_MIO60	C26 MIO60 USB0_D4
PS_MIO61	B29 MIO61 USB0_D5
PS_MIO62	B28 MIO62 USB0_D6
PS_MIO63	A29 MIO63 USB0_D7
PS_MIO64	B30 MIO64 GEM3_TX_CLK
PS_MIO65	D25 MIO65 GEM3_TX_D0
PS_MIO66	C27 MIO66 GEM3_TX_D1
PS_MIO67	C28 MIO67 GEM3_TX_D2
PS_MIO68	C29 MIO68 GEM3_TX_D3
PS_MIO69	D27 MIO69 GEM3_TX_CTL
PS_MIO70	D26 MIO70 GEM3_RX_CLK
PS_MIO71	D30 MIO71 GEM3_RX_D0
PS_MIO72	E27 MIO72 GEM3_RX_D1
PS_MIO73	E30 MIO73 GEM3_RX_D2
PS_MIO74	E29 MIO74 GEM3_RX_D3
PS_MIO75	D29 MIO75 GEM3_RX_CTL
PS_MIO76	E28 MIO76 GEM3_MDC
PS_MIO77	E25 MIO77 GEM3_MDIO

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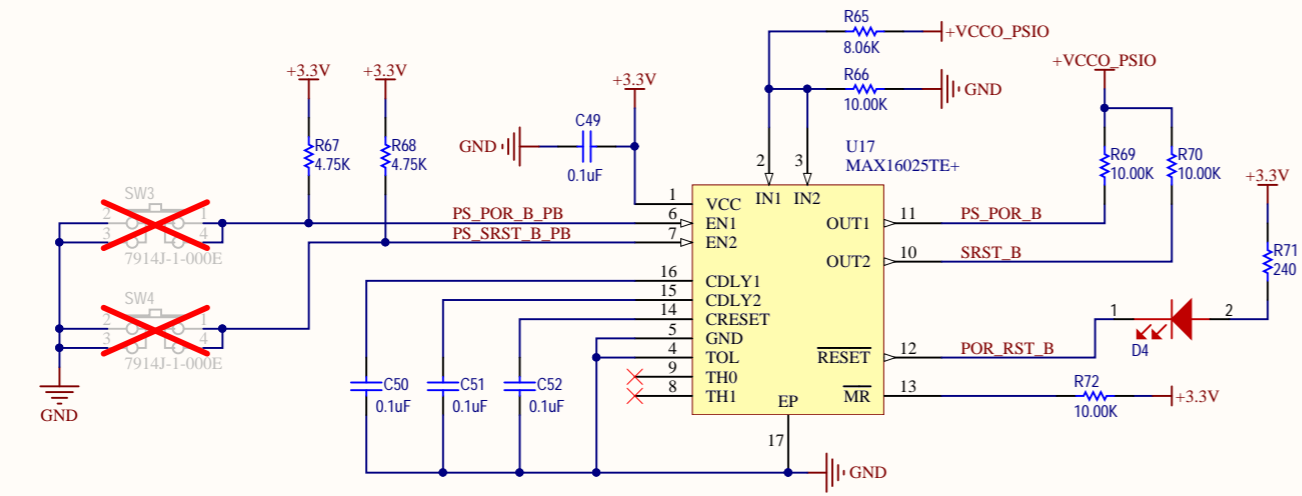
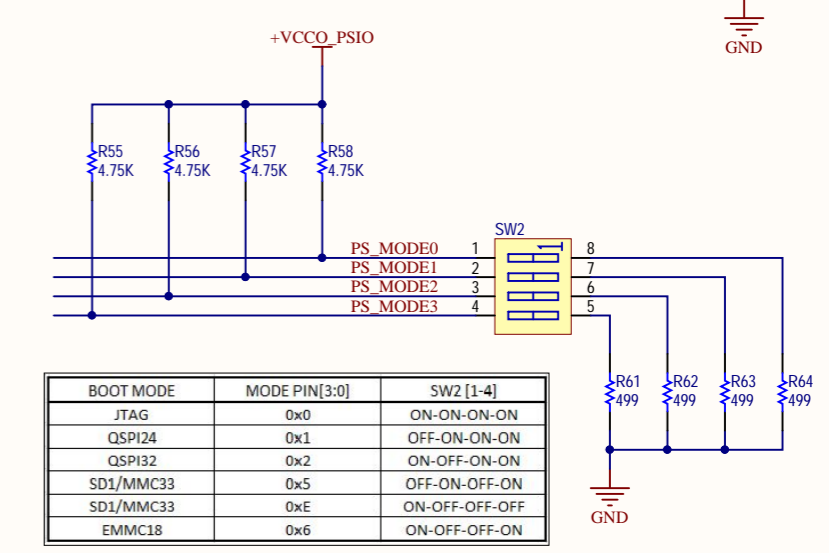
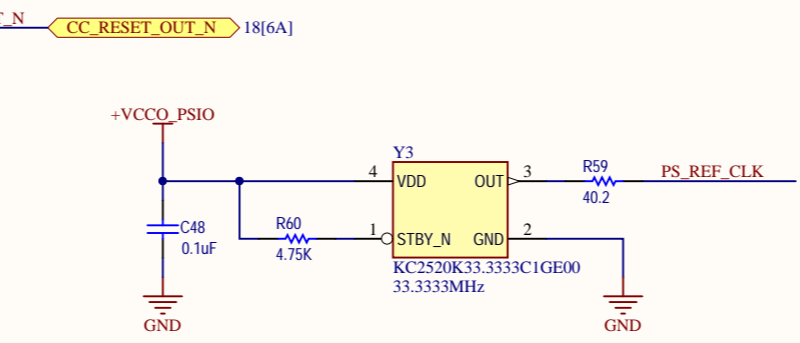
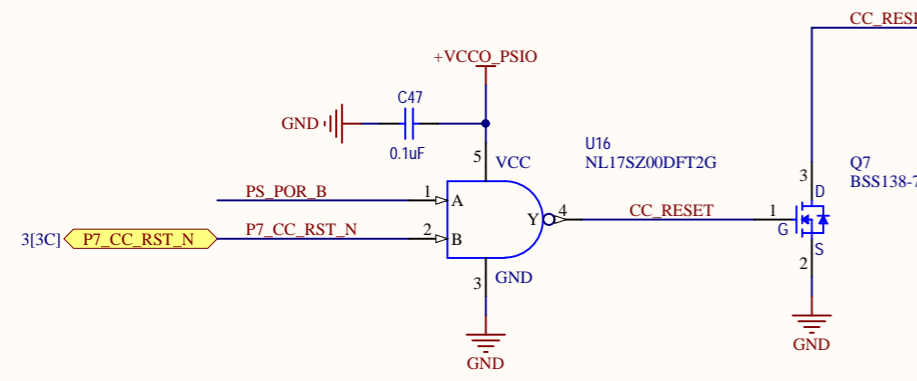
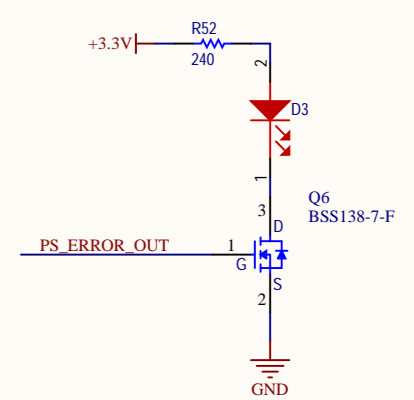
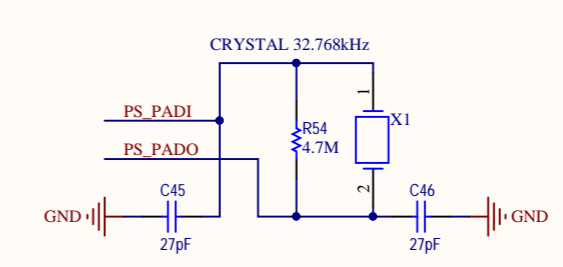
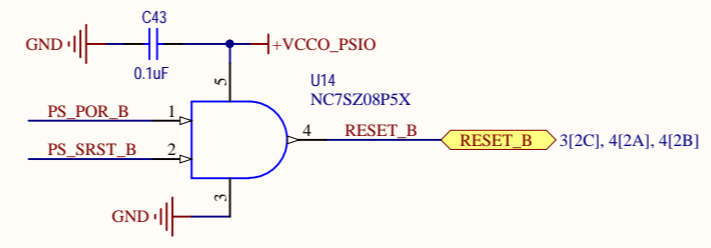
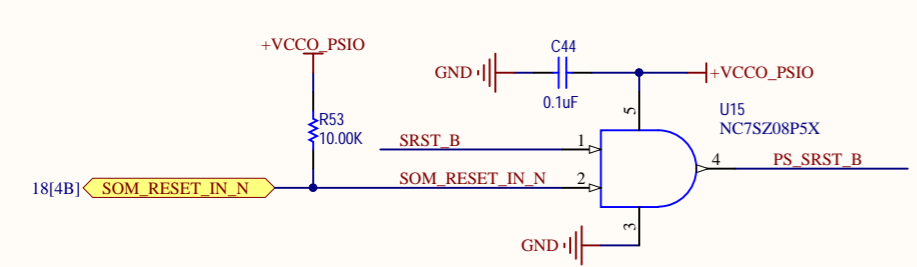
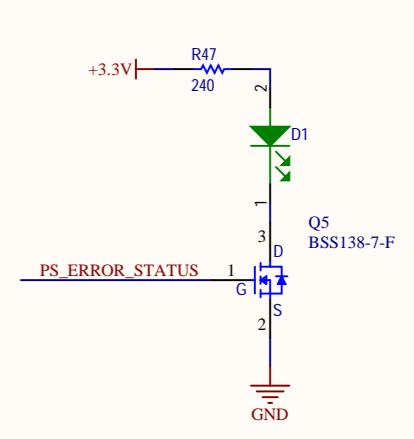
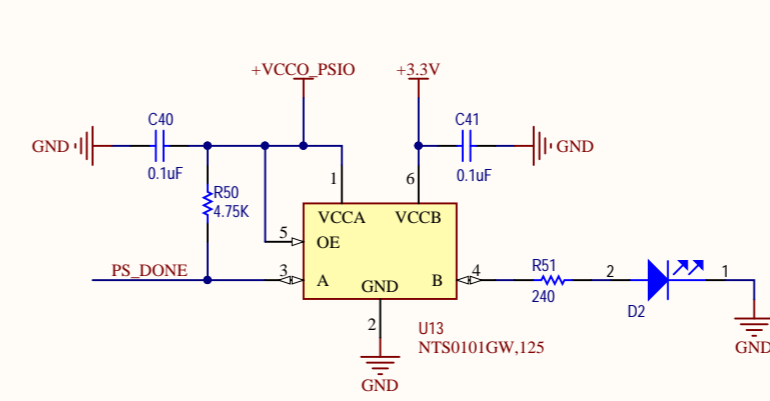
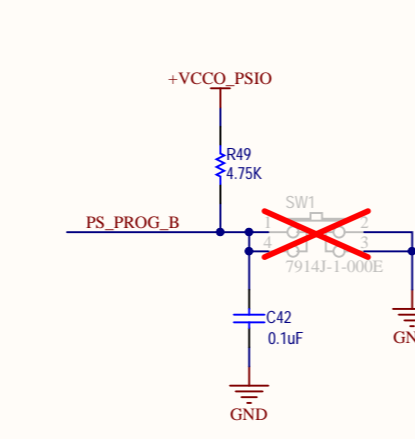
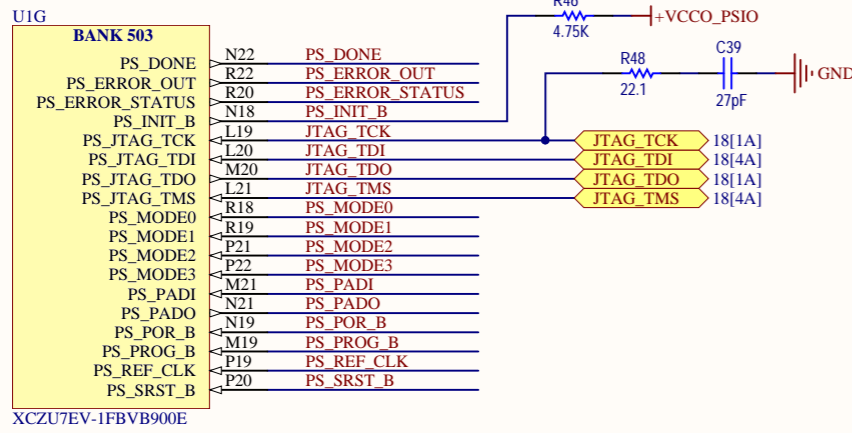


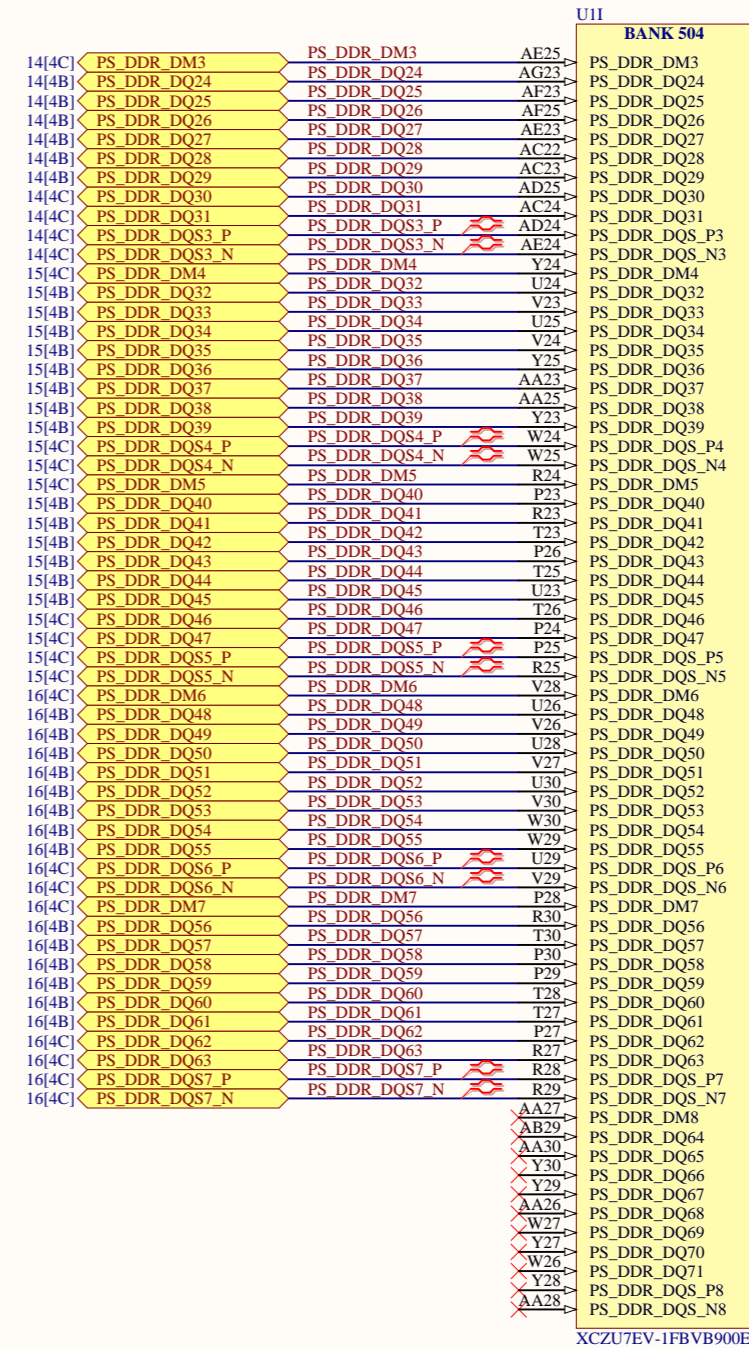
LED FUNCTIONALITY: SW INTERVENTION REQUIRED TO SET DESIRED LED OPERATION. PLEASE SEE 88E1512 DATASHEET.

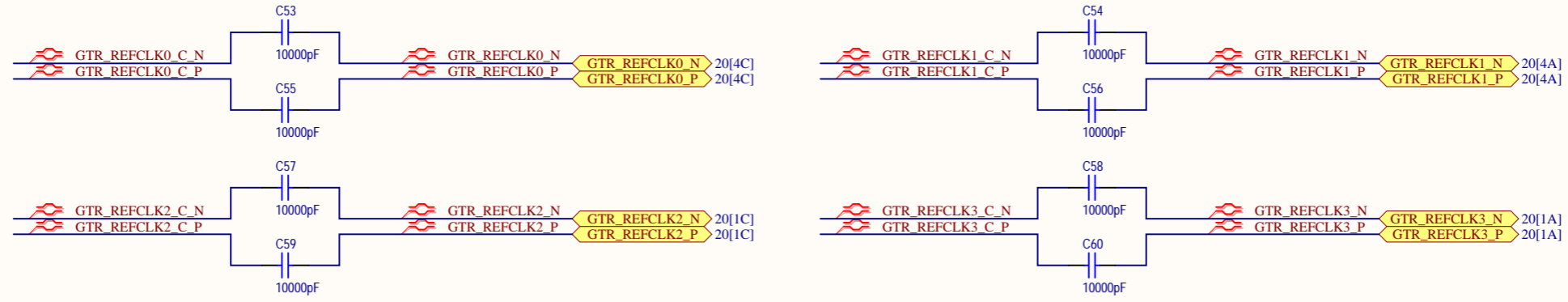
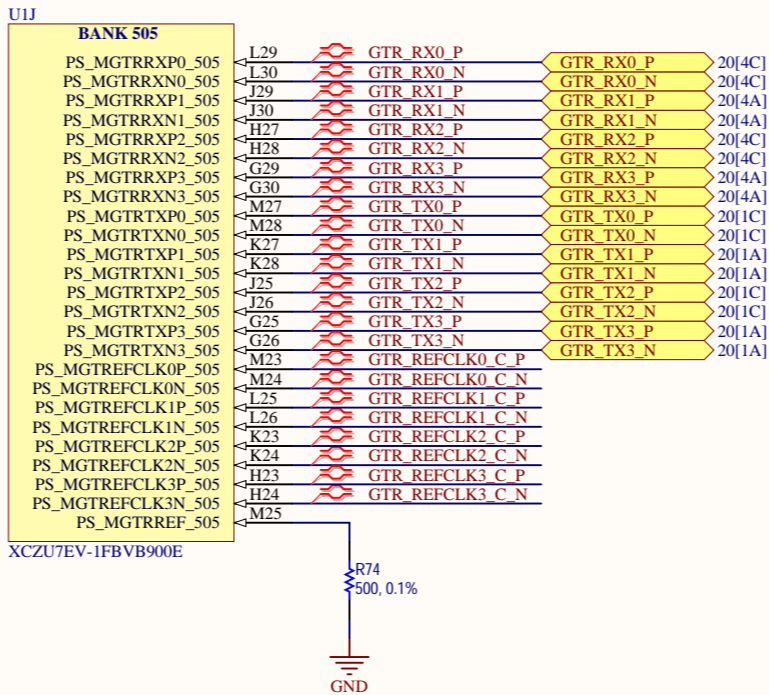
ETH_CONFIG:
GND: PHYAD[0] = 0
VCCO_PSIO: PHYAD[0] = 1

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Doc Num:	SCH-US2SOM	1	01	03
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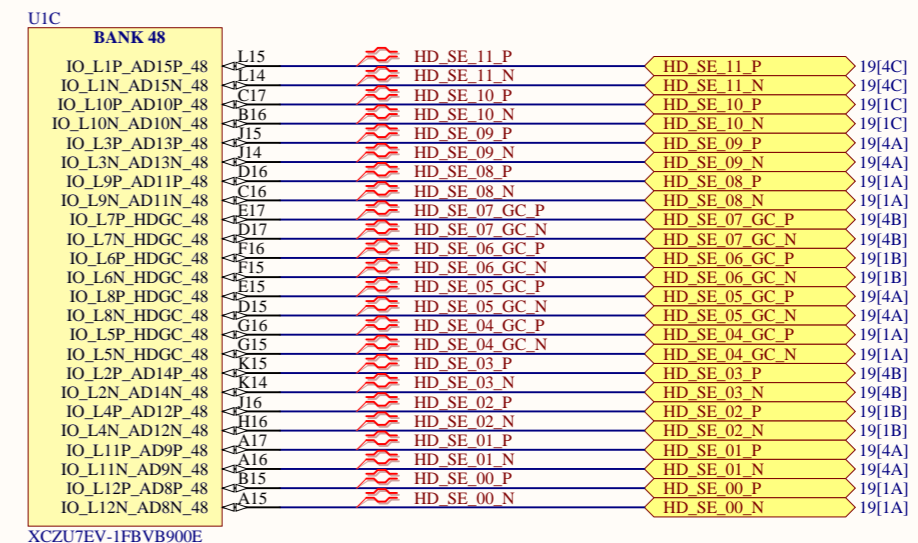
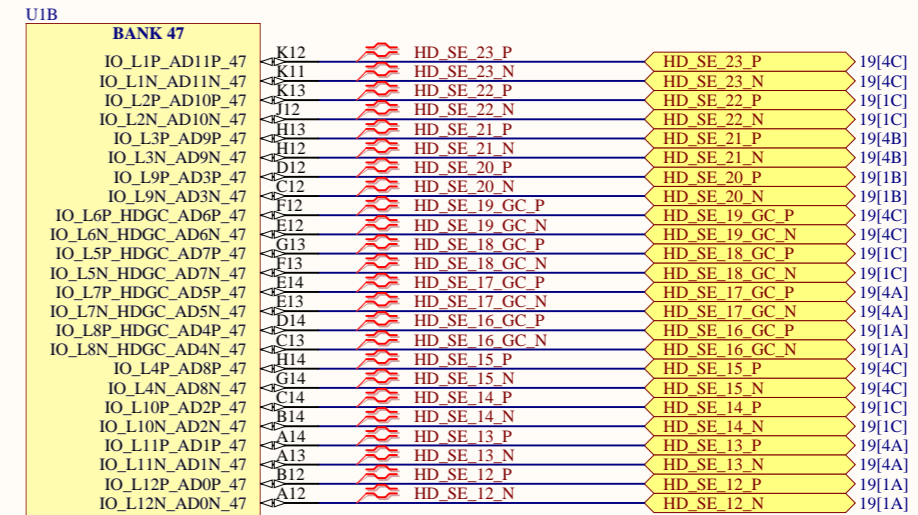
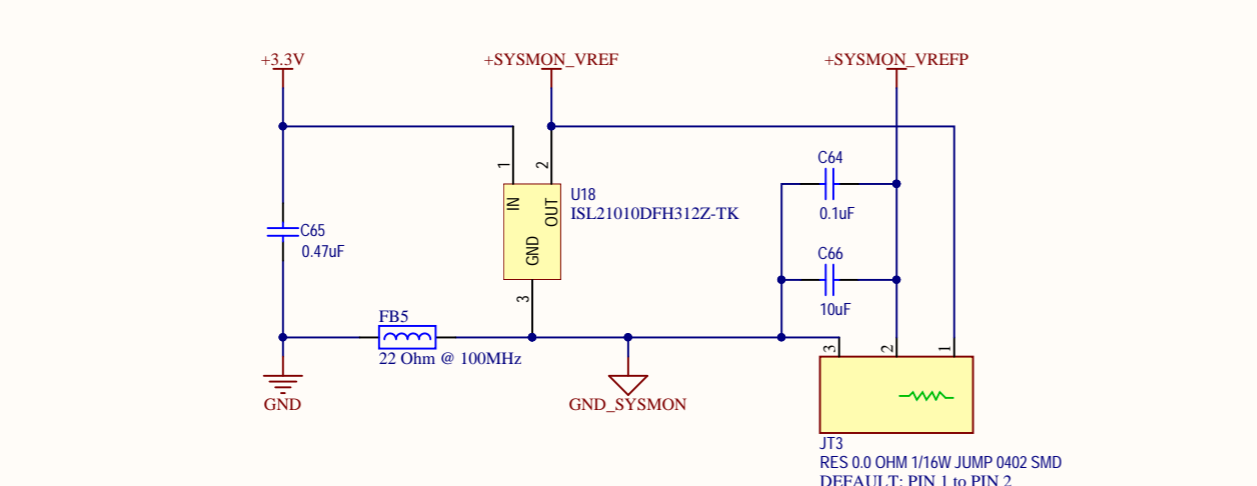
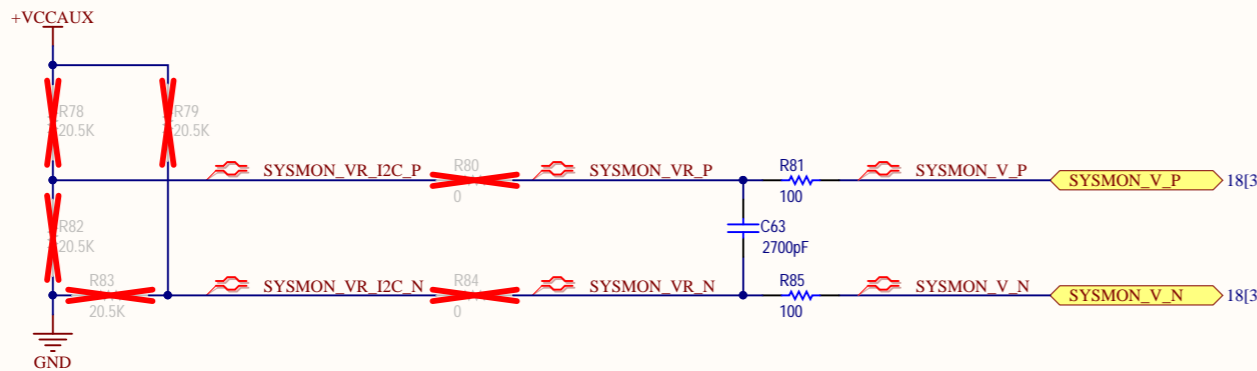
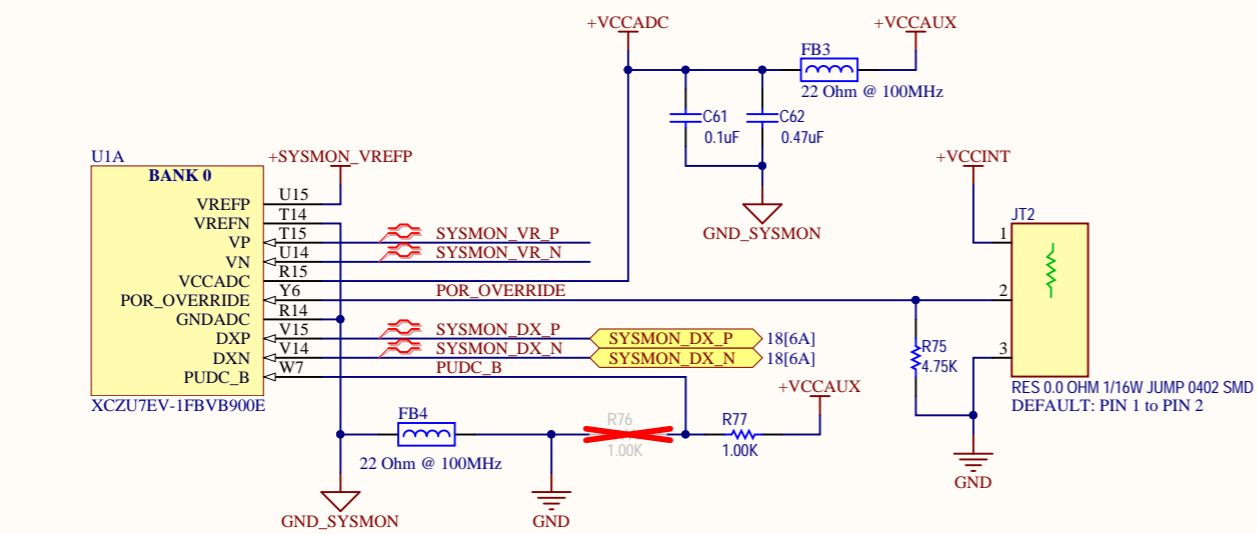






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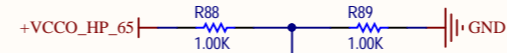




UIK

BANK 64		
VREF_64	AA17	HP DP 23 P
IO_L6P_T0U_N10_AD6P_64	AD15	HP DP 23 P
IO_L6N_T0U_N11_AD6N_64	AA15	HP DP 23 N
IO_L4P_T0U_N6_DBC_AD7P_64	AA14	HP DP 22 P
IO_L4N_T0U_N7_DBC_AD7N_64	AB14	HP DP 22 N
IO_L2P_T0L_N2_64	AE14	HP DP 21 P
IO_L2N_T0L_N3_64	AE13	HP DP 21 N
IO_L3P_T0L_N4_AD15P_64	AC14	HP DP 20 P
IO_L3N_T0L_N5_AD15N_64	AD14	HP DP 20 N
IO_L5P_T0U_N8_AD14P_64	AA15	HP DP 19 P
IO_L5N_T0U_N9_AD14N_64	AA13	HP DP 18 P
IO_L1P_T0L_N0_DBC_64	AB15	HP DP 19 N
IO_L1N_T0L_N1_DBC_64	AB13	HP DP 18 N
IO_L7P_T1L_N0_QBC_AD13P_64	AG13	HP DP 17 P
IO_L7N_T1L_N1_QBC_AD13N_64	AH13	HP DP 17 N
IO_L8P_T1L_N2_AD5P_64	AK13	HP DP 16 P
IO_L8N_T1L_N3_AD5N_64	AK12	HP DP 16 N
IO_L10P_T1U_N6_QBC_AD4P_64	AJ15	HP DP 11 P
IO_L10N_T1U_N7_QBC_AD4N_64	AI15	HP DP 11 N
IO_L9P_T1U_N8_AD12P_64	AI14	HP DP 10 P
IO_L9N_T1U_N5_AD12N_64	AI14	HP DP 10 N
IO_L12P_T1U_N10_GC_64	AF15	HP DP 15 GC P
IO_L12N_T1U_N11_GC_64	AG15	HP DP 15 GC N
IO_L11P_T1U_N8_GC_64	AG14	HP DP 14 GC P
IO_L11N_T1U_N9_GC_64	AH14	HP DP 14 GC N
IO_L14P_T2L_N2_GC_64	AD17	HP DP 13 GC P
IO_L14N_T2L_N3_GC_64	AE17	HP DP 13 GC N
IO_L13P_T2L_N0_GC_QBC_64	AF16	HP DP 12 GC P
IO_L13N_T2L_N1_GC_QBC_64	AF17	HP DP 12 GC N
IO_L15P_T2L_N4_AD11P_64	AC16	HP DP 09 P
IO_L15N_T2L_N5_AD11N_64	AD16	HP DP 09 N
IO_L19P_T3L_N0_DBC_AD9P_64	AG16	HP DP 08 P
IO_L19N_T3L_N1_DBC_AD9N_64	AH16	HP DP 08 N
IO_L22P_T3U_N6_DBC_AD0P_64	AK17	HP DP 07 P
IO_L22N_T3U_N7_DBC_AD0N_64	AK18	HP DP 07 N
IO_L20P_T3L_N2_AD1P_64	AJ16	HP DP 06 P
IO_L20N_T3L_N3_AD1N_64	AK16	HP DP 06 N
IO_L16P_T2U_N6_QBC_AD3P_64	AA16	HP DP 05 P
IO_L16N_T2U_N7_QBC_AD3N_64	AB16	HP DP 05 N
IO_L17P_T2U_N8_AD10P_64	AC17	HP DP 04 P
IO_L17N_T2U_N9_AD10N_64	AC18	HP DP 04 N
IO_L18P_T2U_N10_AD2P_64	AD19	HP DP 03 P
IO_L18N_T2U_N11_AD2N_64	AE19	HP DP 03 N
IO_L21P_T3L_N4_AD8P_64	AH17	HP DP 02 P
IO_L21N_T3L_N5_AD8N_64	AJ17	HP DP 02 N
IO_L24P_T3U_N10_64	AE18	HP DP 01 P
IO_L24N_T3U_N11_64	AF18	HP DP 01 N
IO_L23P_T3U_N8_64	AG18	HP DP 00 P
IO_L23N_T3U_N9_64	AH18	HP DP 00 N
IO_T1U_N12_64	AF13	HP SE 00
IO_T1U_N12_64	AG19	HP SE 01
IO_T0U_N12_VRP_64	AC13	HP SE 02
IO_T2U_N12_64	AC19	HP SE 03

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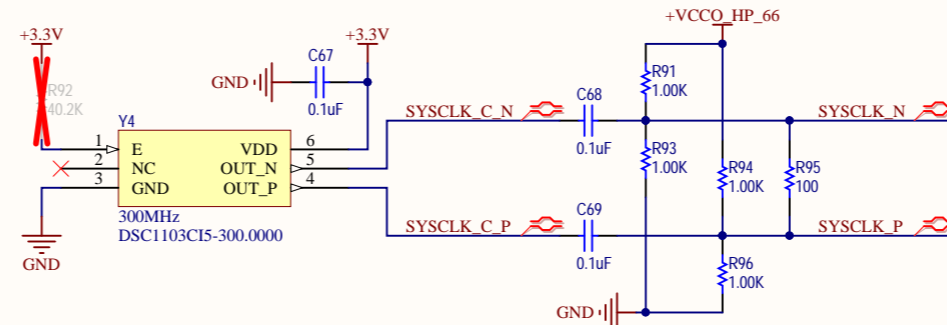
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VREF_65	AE12	HP DP 47 P
IO_L22P_T3U_N6_DBC_AD0P_65	AG4	HP DP 47 N
IO_L22N_T3U_N7_DBC_AD0N_65	AG3	HP DP 47 N
IO_L23P_T3U_N8_I2C_SCLK_65	AG1	HP DP 46 P
IO_L23N_T3U_N9_65	AH1	HP DP 46 N
IO_L19P_T3L_N0_DBC_AD9P_65	AK3	HP DP 45 P
IO_L19N_T3L_N1_DBC_AD9N_65	AK2	HP DP 45 N
IO_L21P_T3L_N4_AD8P_65	AH3	HP DP 44 P
IO_L21N_T3L_N5_AD8N_65	AH2	HP DP 44 N
IO_L10P_T1U_N6_QBC_AD4P_65	AE8	HP DP 43 N
IO_L10N_T1U_N7_QBC_AD4N_65	AE9	HP DP 43 P
IO_L1P_T0L_N0_DBC_65	AH12	HP DP 42 P
IO_L1N_T0L_N1_DBC_65	AJ12	HP DP 42 N
IO_L3P_T0L_N4_AD15P_65	AG11	HP DP 41 P
IO_L3N_T0L_N5_AD15N_65	AH11	HP DP 41 N
IO_L8P_T1L_N2_AD5P_65	AH9	HP DP 40 P
IO_L8N_T1L_N3_AD5N_65	AJ9	HP DP 40 N
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	AF3	HP DP 39 P
IO_L24N_T3U_N11_PERSTN0_65	AF2	HP DP 39 N
IO_L20P_T3L_N2_AD1P_65	AJ2	HP DP 38 P
IO_L20N_T3L_N3_AD1N_65	AJ1	HP DP 38 N
IO_L11P_T1U_N8_GC_65	AG8	HP DP 35 GC P
IO_L11N_T1U_N9_GC_65	AH8	HP DP 35 GC N
IO_L12P_T1U_N10_GC_65	AH7	HP DP 34 GC P
IO_L12N_T1U_N11_GC_65	AJ7	HP DP 34 GC N
IO_L13P_T2L_N0_GC_QBC_65	AH6	HP DP 33 GC P
IO_L13N_T2L_N1_GC_QBC_65	AJ6	HP DP 33 GC N
IO_L14P_T2L_N2_GC_65	AG6	HP DP 32 GC P
IO_L14N_T2L_N3_GC_65	AG5	HP DP 32 GC N
IO_L17P_T2U_N8_AD10P_65	AJ4	HP DP 37 P
IO_L17N_T2U_N9_AD10N_65	AK4	HP DP 37 N
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	AJ11	HP DP 36 P
IO_L4N_T0U_N7_DBC_AD7N_65	AK11	HP DP 36 N
IO_L7P_T1L_N0_QBC_AD13P_65	AK9	HP DP 31 P
IO_L7N_T1L_N1_QBC_AD13N_65	AK8	HP DP 31 N
IO_L18P_T2U_N10_AD2P_65	AF6	HP DP 30 P
IO_L18N_T2U_N11_AD2N_65	AF5	HP DP 30 N
IO_L15P_T2L_N4_AD11P_65	AK7	HP DP 29 P
IO_L15N_T2L_N5_AD11N_65	AK6	HP DP 29 N
IO_L16P_T2U_N6_QBC_AD3P_65	AJ5	HP DP 28 P
IO_L16N_T2U_N7_QBC_AD3N_65	AK5	HP DP 28 N
IO_L2P_T0L_N2_65	AF12	HP DP 27 P
IO_L2N_T0L_N3_65	AF11	HP DP 27 N
IO_L9P_T1L_N4_AD12P_65	AF8	HP DP 26 P
IO_L9N_T1L_N5_AD12N_65	AF7	HP DP 26 N
IO_L5P_T0U_N8_AD14P_65	AJ10	HP DP 25 P
IO_L5N_T0U_N9_AD14N_65	AK10	HP DP 25 N
IO_L6P_T0U_N10_AD6P_65	AF10	HP DP 24 P
IO_L6N_T0U_N11_AD6N_65	AG10	HP DP 24 N
IO_T3U_N12_65	AF1	HP SE 04
IO_T3U_N12_65	AH4	HP SE 05
IO_T2U_N12_65	AG9	HP SE 06
IO_T1U_N12_65	AE10	HP SE 07

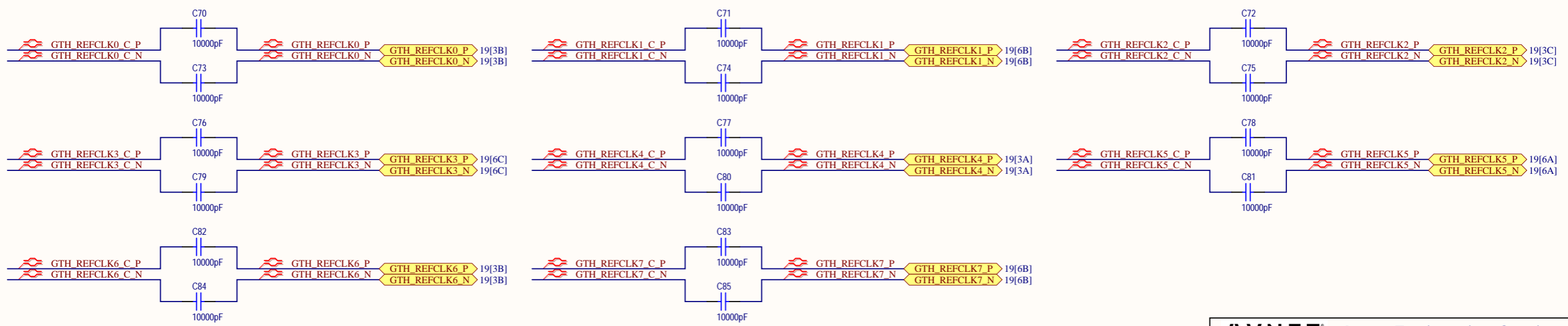
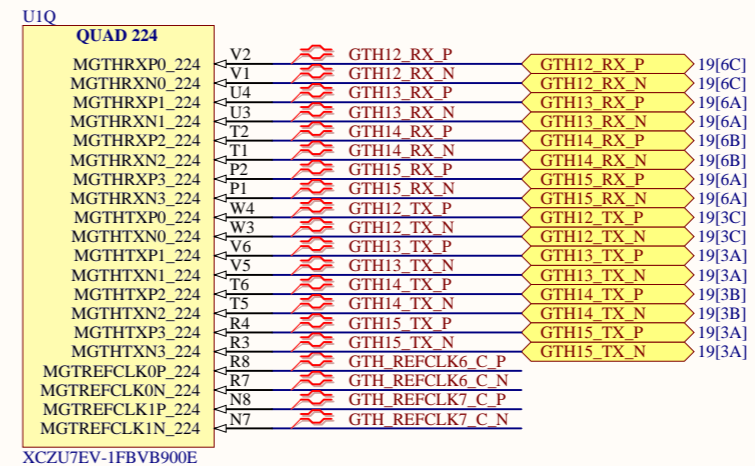
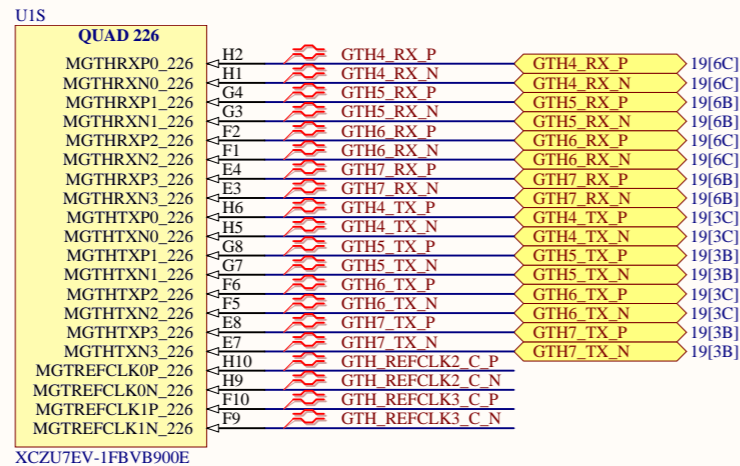
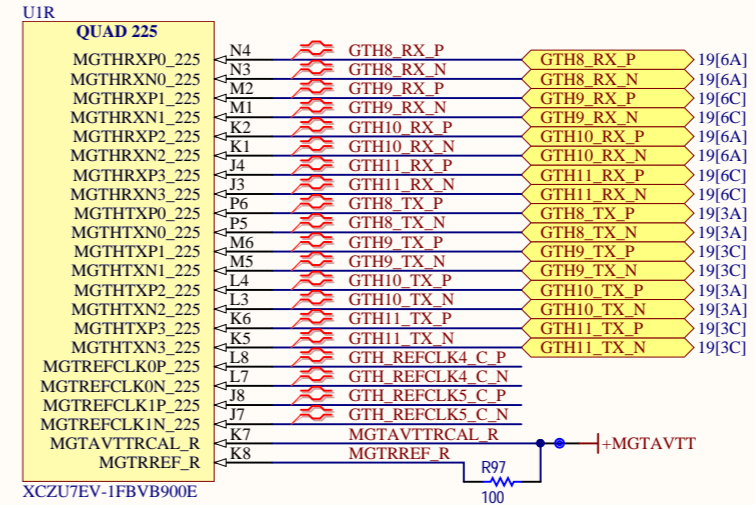
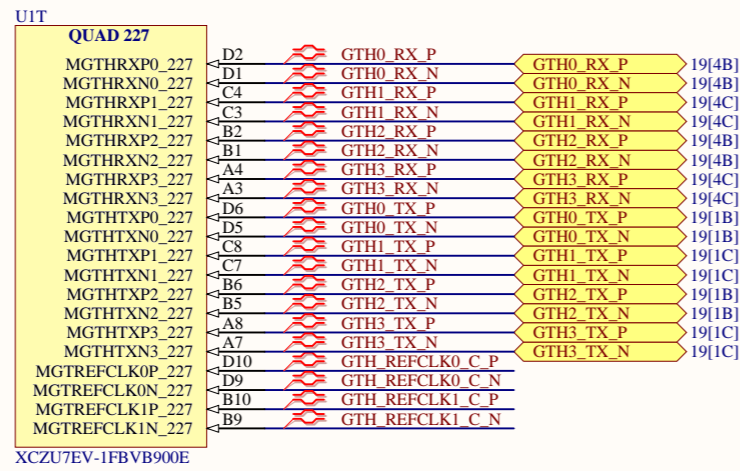
XCZU7EV-1FBVB900E

UIM

BANK 66		
VREF_66	W10	PL_DDR4_A9
IO_L1P_T0L_N0_DBC_66	AC12	PL_DDR4_A10
IO_L1N_T0L_N1_DBC_66	AD12	PL_DDR4_A11
IO_L2P_T0L_N2_66	AA12	PL_DDR4_A12
IO_L2N_T0L_N3_66	AA11	PL_DDR4_A13
IO_L3P_T0L_N4_AD15P_66	AB11	PL_DDR4_WE_N
IO_L3N_T0L_N5_AD15N_66	AC11	PL_DDR4_CAS_N
IO_L4P_T0U_N6_DBC_AD7P_66	AD11	PL_DDR4_RAS_N
IO_L4N_T0U_N7_DBC_AD7N_66	AD10	PL_DDR4_RAS_N
IO_L5P_T0U_N8_AD14P_66	AB10	PL_DDR4_BA1
IO_L5N_T0U_N9_AD14N_66	AB9	PL_DDR4_BA0
IO_L6P_T0U_N10_AD6P_66	Y10	PL_DDR4_BG
IO_L6N_T0U_N11_AD6N_66	AA10	PL_DDR4_CS_N
IO_L7P_T1L_N0_QBC_AD13P_66	AC9	PL_DDR4_A0
IO_L7N_T1L_N1_QBC_AD13N_66	AD9	PL_DDR4_A1
IO_L8P_T1L_N2_AD5P_66	AC6	PL_DDR4_A2
IO_L8N_T1L_N3_AD5N_66	AD6	PL_DDR4_A3
IO_L9P_T1L_N4_AD12P_66	W8	PL_DDR4_A4
IO_L9N_T1L_N5_AD12N_66	Y8	PL_DDR4_A5
IO_L10P_T1U_N6_QBC_AD4P_66	Y7	PL_DDR4_CK_P
IO_L10N_T1U_N7_QBC_AD4N_66	AA7	PL_DDR4_CK_N
IO_L11P_T1U_N8_GC_66	AC8	PL_DDR4_CK_N
IO_L11N_T1U_N9_GC_66	AC7	PL_DDR4_CK_N
IO_L12P_T1U_N10_GC_66	AA8	PL_DDR4_A6
IO_L12N_T1U_N11_GC_66	AB8	PL_DDR4_A7
IO_L13P_T2L_N0_GC_QBC_66	AD7	PL_DDR4_DM_DBI_1_N
IO_L13N_T2L_N1_GC_QBC_66	AE7	PL_DDR4_CKE
IO_L14P_T2L_N2_GC_66	AB6	PL_DDR4_DQ8
IO_L14N_T2L_N3_GC_66	AB5	PL_DDR4_DQ9
IO_L15P_T2L_N4_AD11P_66	AD5	PL_DDR4_DQ10
IO_L15N_T2L_N5_AD11N_66	AE5	PL_DDR4_DQ11
IO_L16P_T2U_N6_QBC_AD3P_66	AD4	PL_DDR4_DQS1_P
IO_L16N_T2U_N7_QBC_AD3N_66	AE4	PL_DDR4_DQS1_N
IO_L17P_T2U_N8_AD10P_66	AB4	PL_DDR4_DQ12
IO_L17N_T2U_N9_AD10N_66	AC4	PL_DDR4_DQ13
IO_L18P_T2U_N10_AD2P_66	AA6	PL_DDR4_DQ14
IO_L18N_T2U_N11_AD2N_66	AA5	PL_DDR4_DQ15
IO_L19P_T3L_N0_DBC_AD9P_66	AD2	PL_DDR4_DM_DBI_0_N
IO_L19N_T3L_N1_DBC_AD9N_66	AE2	PL_DDR4_ACT_N
IO_L20P_T3L_N2_AD1P_66	AD1	PL_DDR4_DQ0
IO_L20N_T3L_N3_AD1N_66	AE1	PL_DDR4_DQ1
IO_L21P_T3L_N4_AD8P_66	AC3	PL_DDR4_DQ2
IO_L21N_T3L_N5_AD8N_66	AA3	PL_DDR4_DQ3
IO_L22P_T3U_N6_DBC_AD0P_66	AB3	PL_DDR4_DQS0_P
IO_L22N_T3U_N7_DBC_AD0N_66	AB1	PL_DDR4_DQS0_N
IO_L23P_T3U_N8_66	AB1	PL_DDR4_DQ4
IO_L23N_T3U_N9_66	AC1	PL_DDR4_DQ5
IO_L24P_T3U_N10_66	AA2	PL_DDR4_DQ6
IO_L24N_T3U_N11_66	AA1	PL_DDR4_DQ7
IO_T0U_N12_VRP_66	Y9	PL_DDR4_A8
IO_T1U_N12_66	W9	PL_DDR4_ODT
IO_T2U_N12_66	AE3	PL_DDR4_ODT
IO_T3U_N12_66	Y1	PL_DDR4_RESET_N

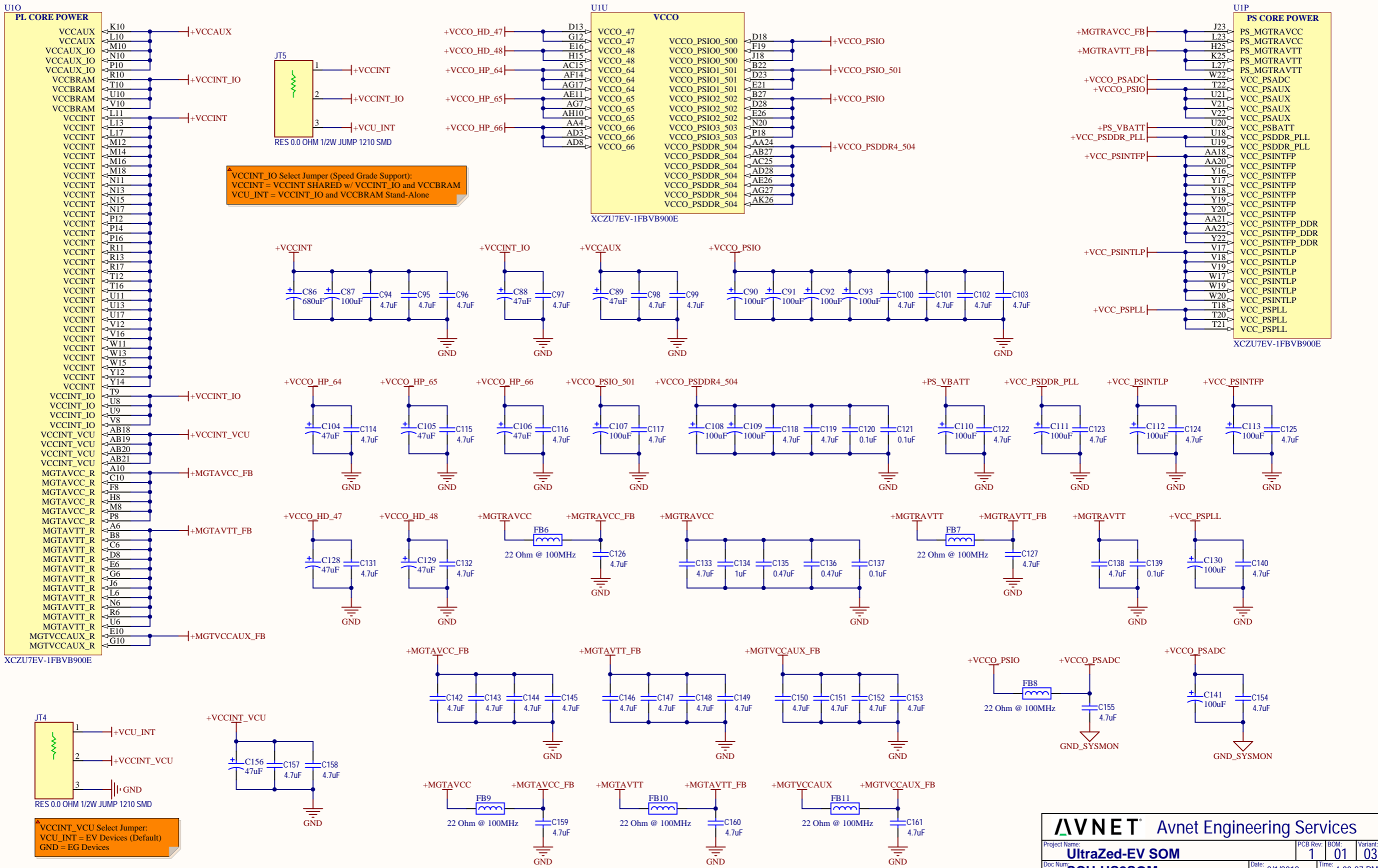
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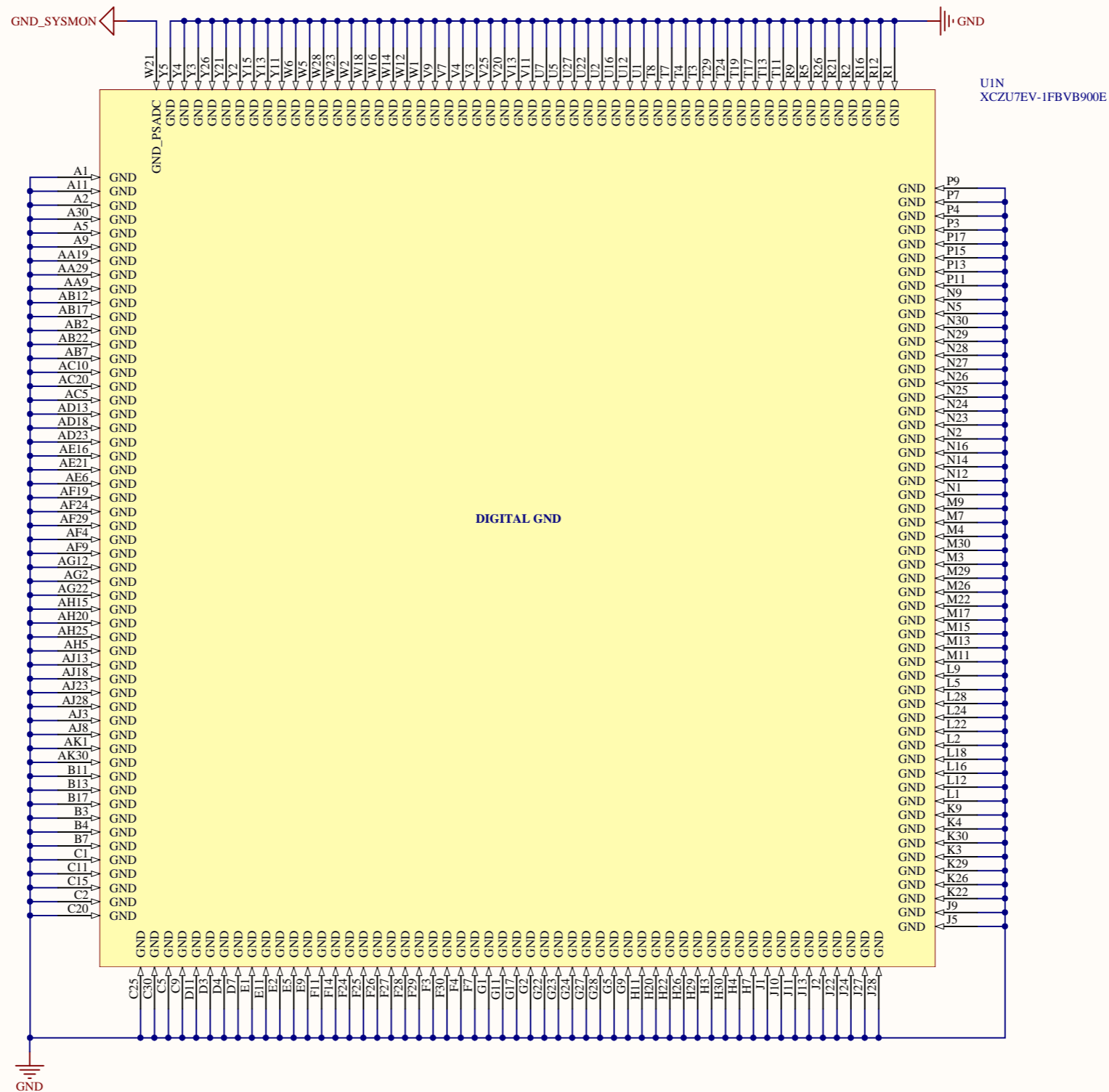
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Doc Num:	SCH-US2SOM	1	01	03
Sheet Title:	10 - MPSoc GTH MGT Quads.SchDoc	Date:	2/1/2018	Time:
			4:00:26 PM	
Sheet:	B	Size:	10 of 25	Sheet:



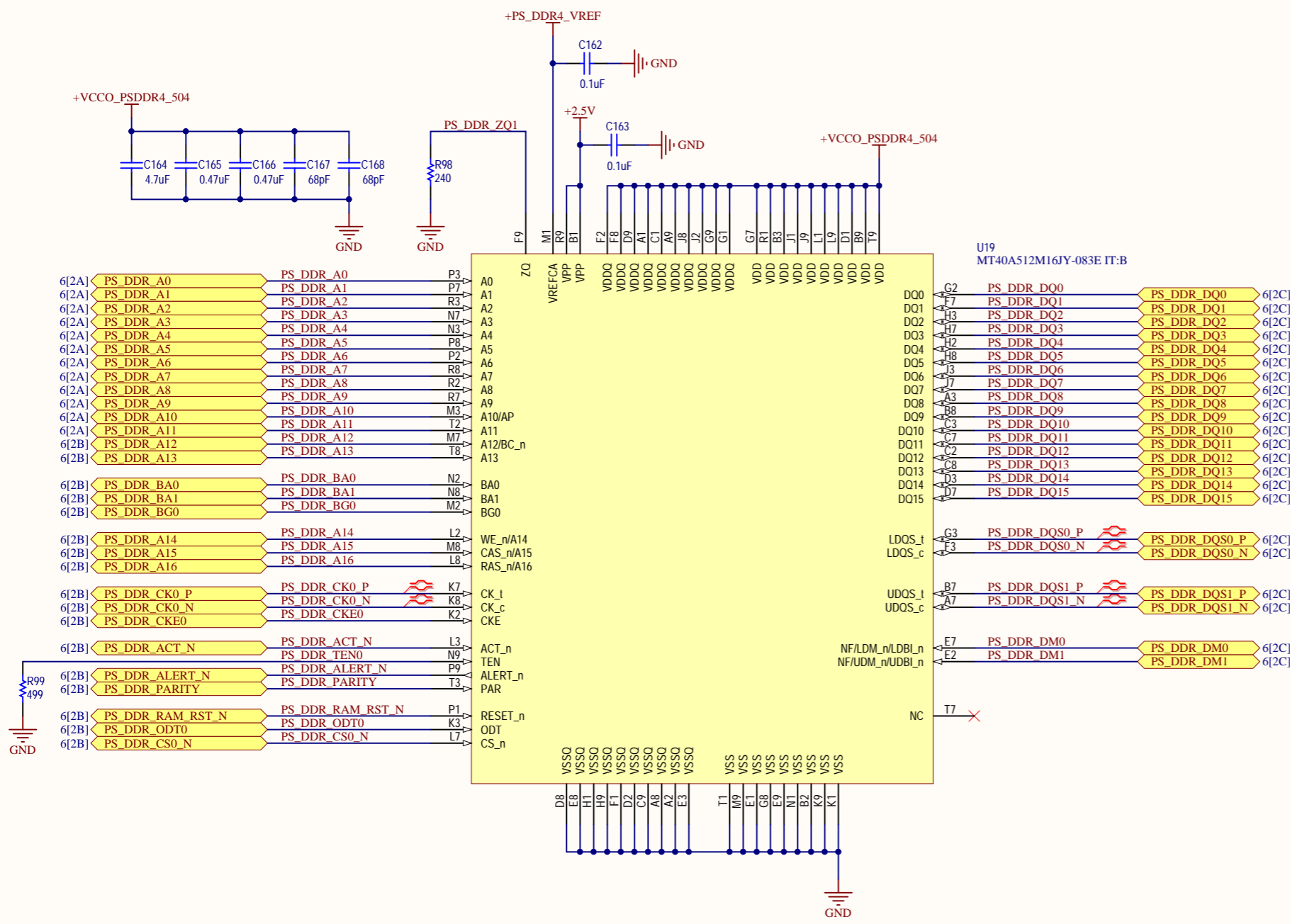
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VCCINT = VCCINT SHARED w/ VCCINT_IO and VCCBRAM
VCU_INT = VCCINT_IO and VCCBRAM Stand-Alone

VCCINT_VCU Select Jumper:
VCU_INT = EV Devices (Default)
GND = EG Devices

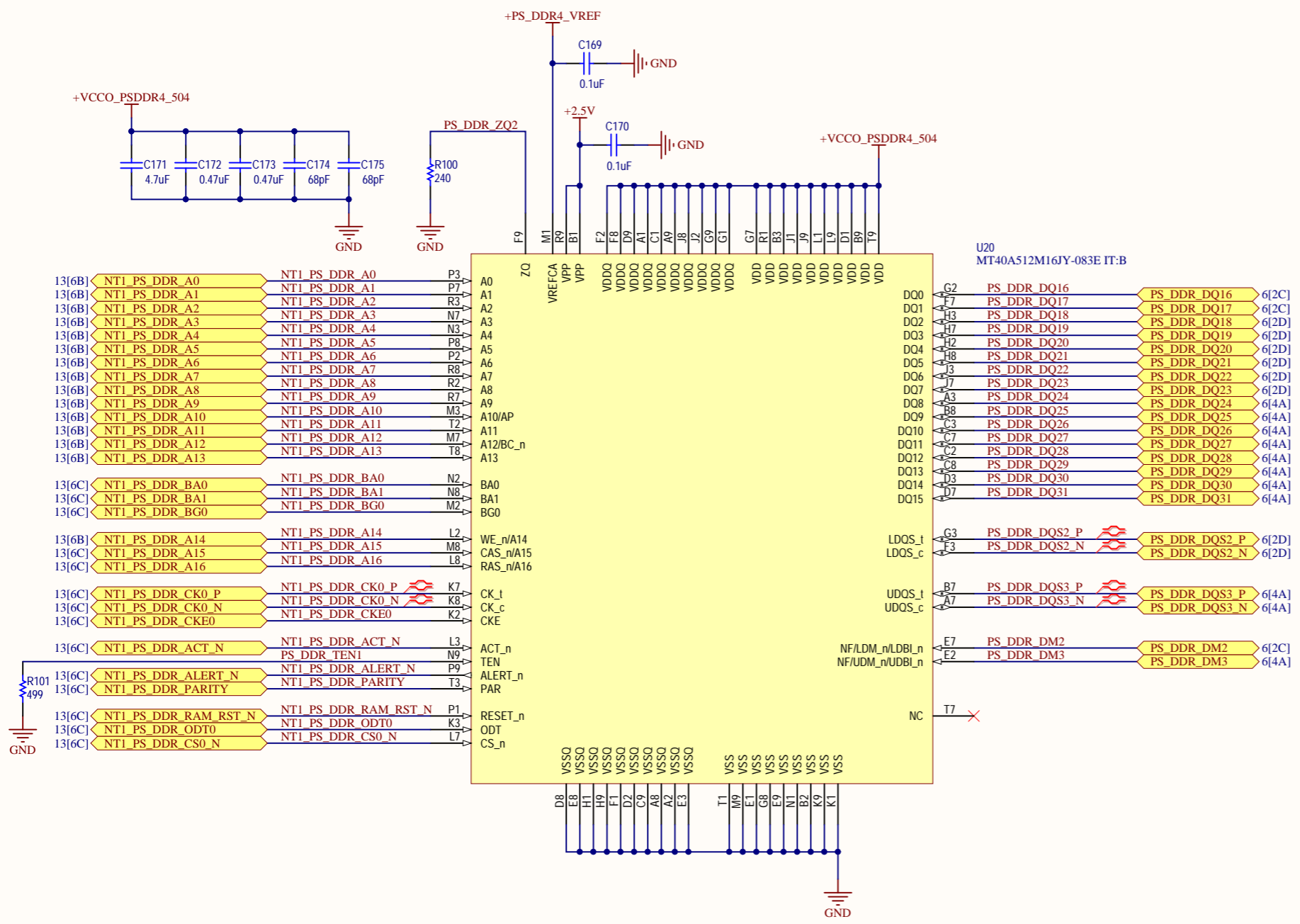
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Doc Num:	SCH-US2SOM	1	01	03
Date:	2/1/2018	Time:	4:00:27 PM	
Sheet Title:	11 - MPSoc Power and Decoupling.SchDoc	Size:	B	Sheet: 11 of 25



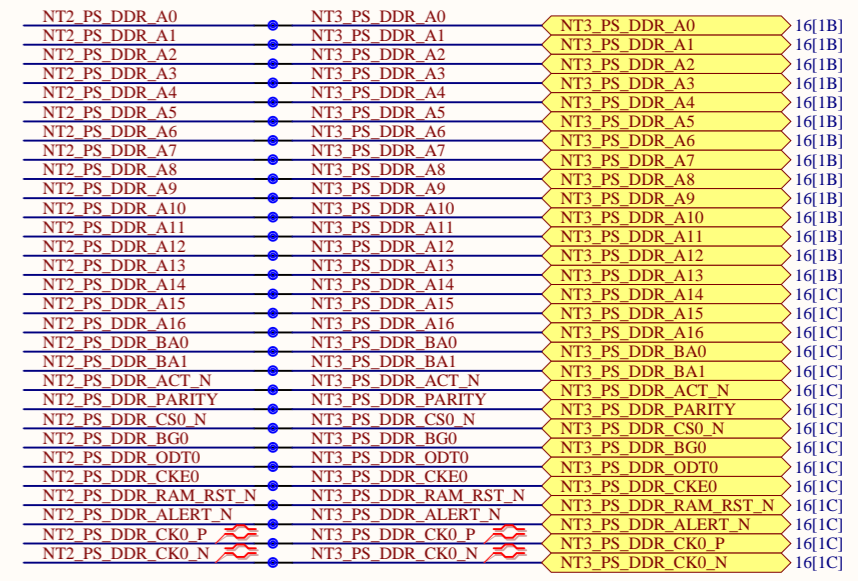
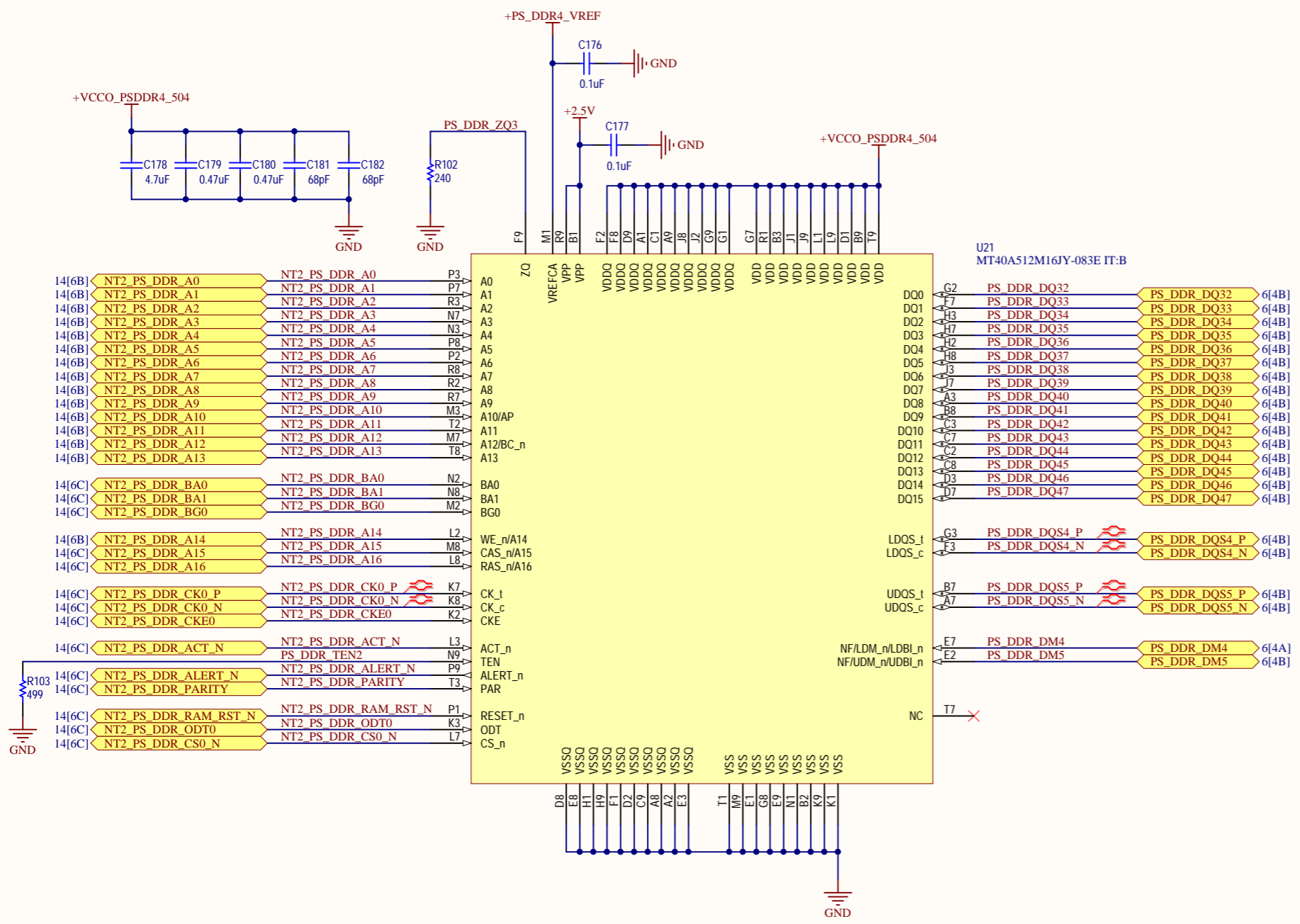
AVNET Avnet Engineering Services			
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Doc Num:	SCH-US2SOM	BOM:	01
Sheet Title:	12 - MPSoC Ground.SchDoc	Variant:	03
Date:	2/1/2018	Time:	4:00:28 PM
Size:	B	Sheet:	12 of 25

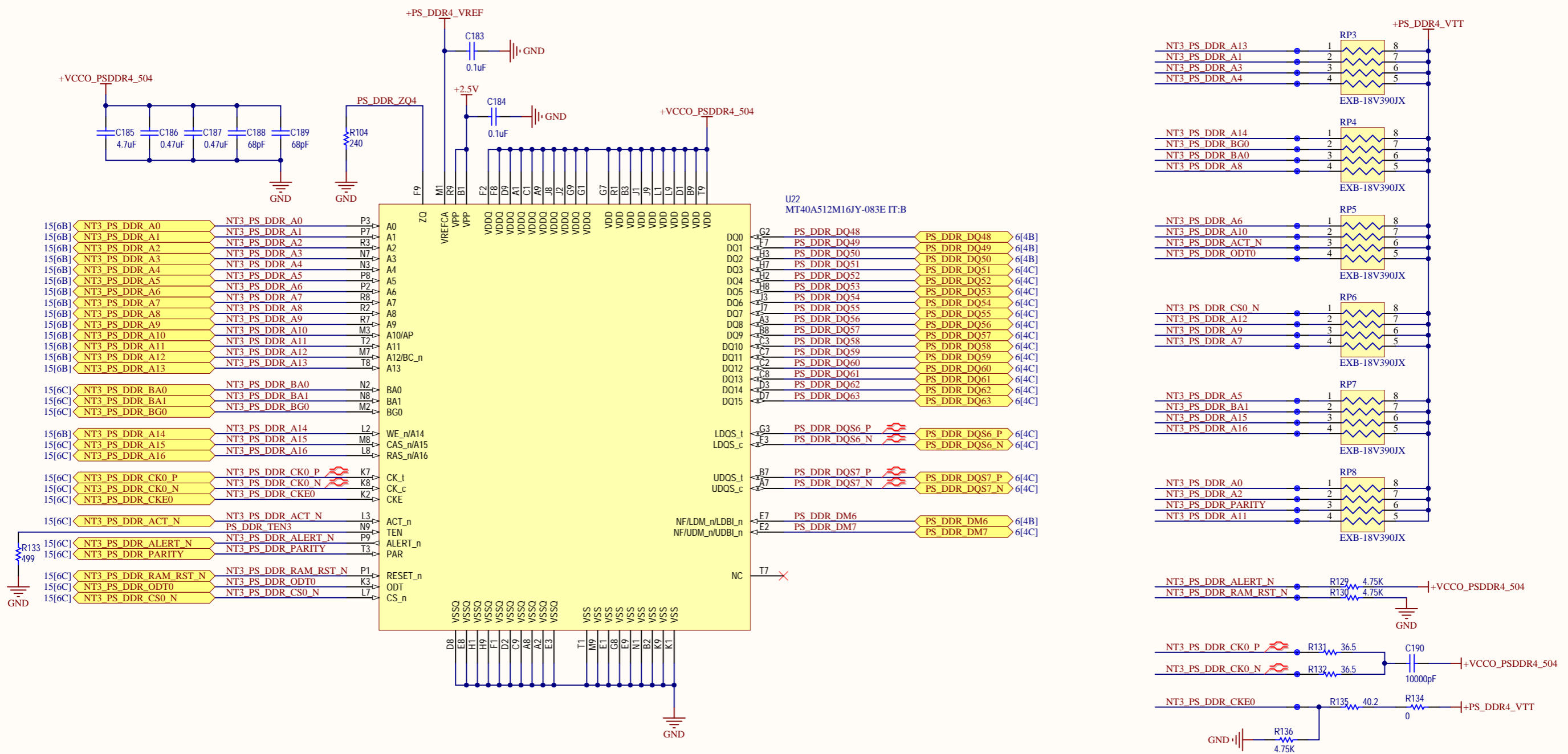


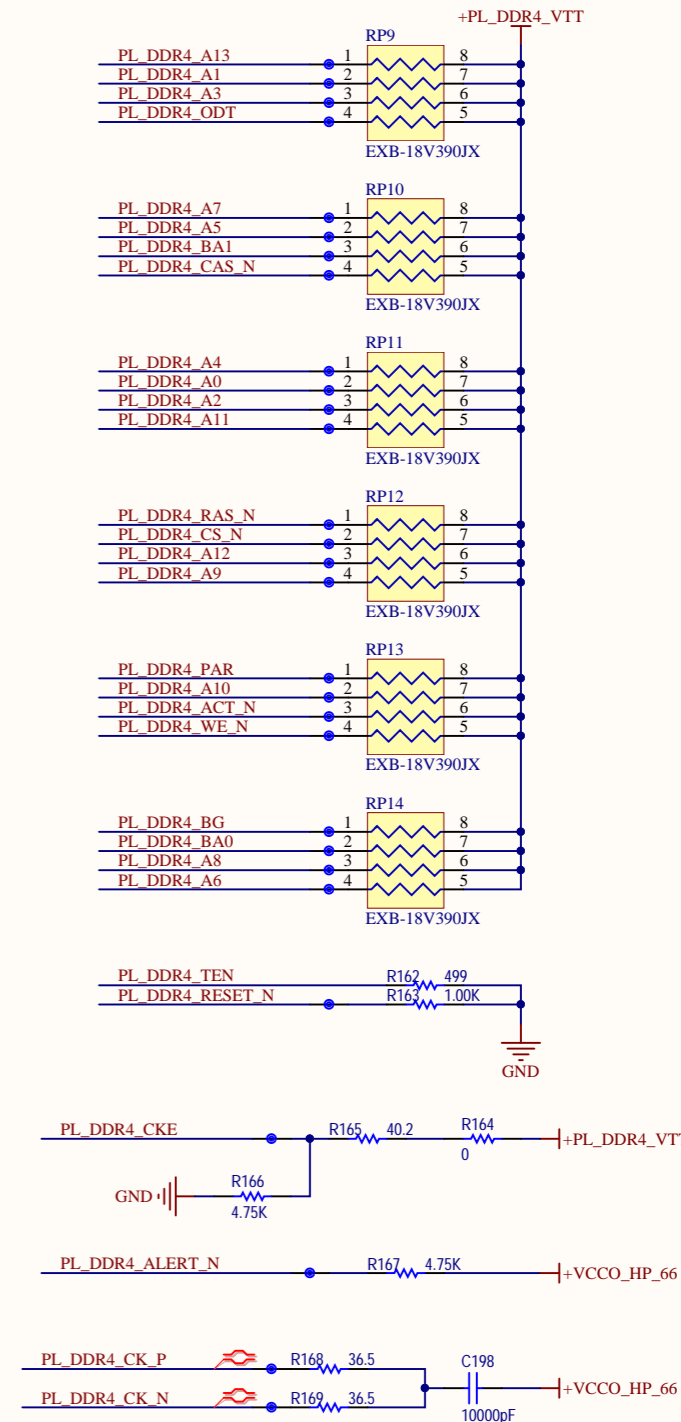
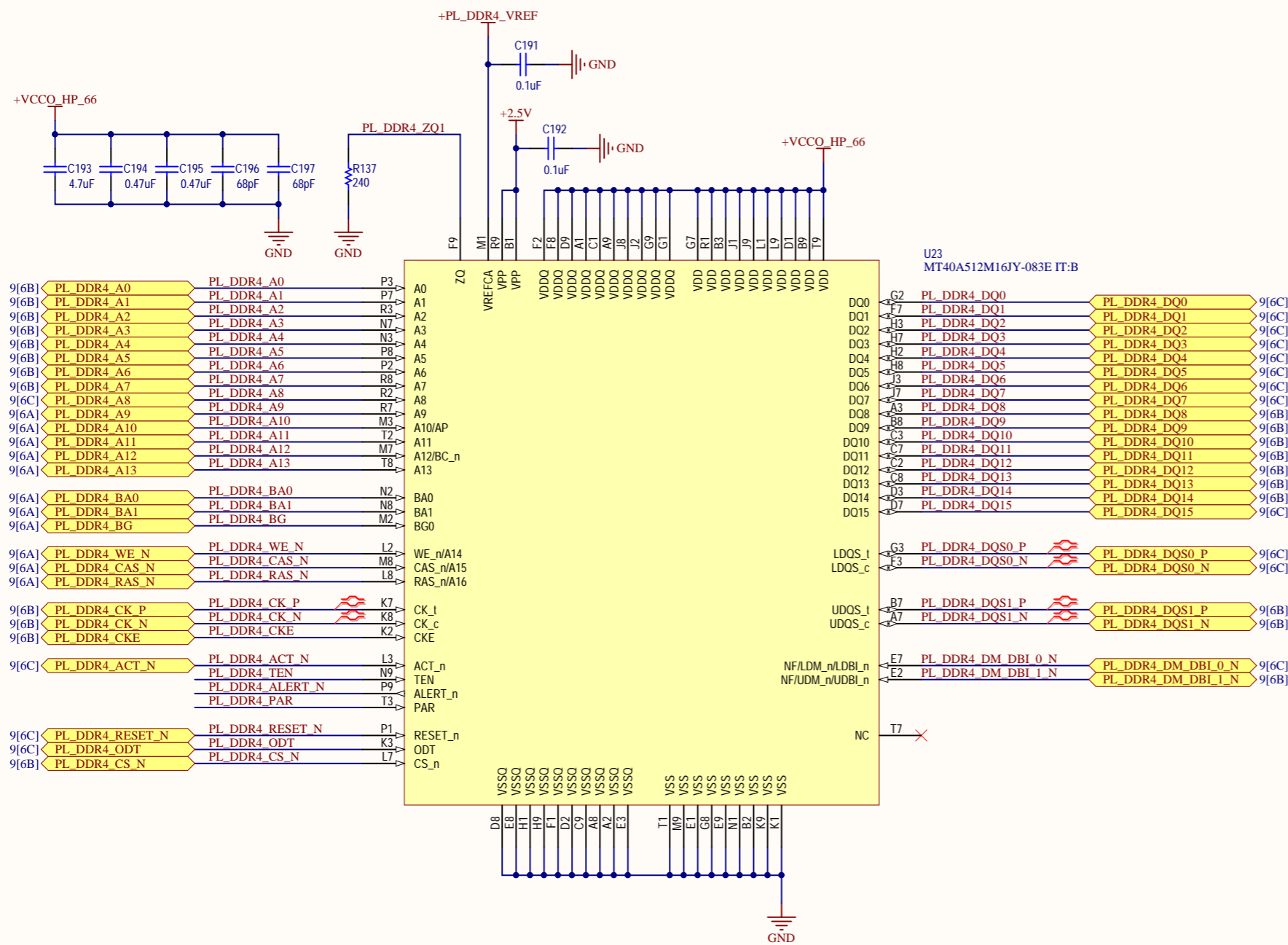
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PS_DDR_A2	NT1_PS_DDR_A2	NT1_PS_DDR_A2	14[1B]
PS_DDR_A3	NT1_PS_DDR_A3	NT1_PS_DDR_A3	14[1B]
PS_DDR_A4	NT1_PS_DDR_A4	NT1_PS_DDR_A4	14[1B]
PS_DDR_A5	NT1_PS_DDR_A5	NT1_PS_DDR_A5	14[1B]
PS_DDR_A6	NT1_PS_DDR_A6	NT1_PS_DDR_A6	14[1B]
PS_DDR_A7	NT1_PS_DDR_A7	NT1_PS_DDR_A7	14[1B]
PS_DDR_A8	NT1_PS_DDR_A8	NT1_PS_DDR_A8	14[1B]
PS_DDR_A9	NT1_PS_DDR_A9	NT1_PS_DDR_A9	14[1B]
PS_DDR_A10	NT1_PS_DDR_A10	NT1_PS_DDR_A10	14[1B]
PS_DDR_A11	NT1_PS_DDR_A11	NT1_PS_DDR_A11	14[1B]
PS_DDR_A12	NT1_PS_DDR_A12	NT1_PS_DDR_A12	14[1B]
PS_DDR_A13	NT1_PS_DDR_A13	NT1_PS_DDR_A13	14[1B]
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PS_DDR_A15	NT1_PS_DDR_A15	NT1_PS_DDR_A15	14[1C]
PS_DDR_A16	NT1_PS_DDR_A16	NT1_PS_DDR_A16	14[1C]
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PS_DDR_BA1	NT1_PS_DDR_BA1	NT1_PS_DDR_BA1	14[1C]
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PS_DDR_PARITY	NT1_PS_DDR_PARITY	NT1_PS_DDR_PARITY	14[1C]
PS_DDR_CS0_N	NT1_PS_DDR_CS0_N	NT1_PS_DDR_CS0_N	14[1C]
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PS_DDR_RAM_RST_N	NT1_PS_DDR_RAM_RST_N	NT1_PS_DDR_RAM_RST_N	14[1C]
PS_DDR_ALERT_N	NT1_PS_DDR_ALERT_N	NT1_PS_DDR_ALERT_N	14[1C]
PS_DDR_CK0_P	NT1_PS_DDR_CK0_P	NT1_PS_DDR_CK0_P	14[1C]
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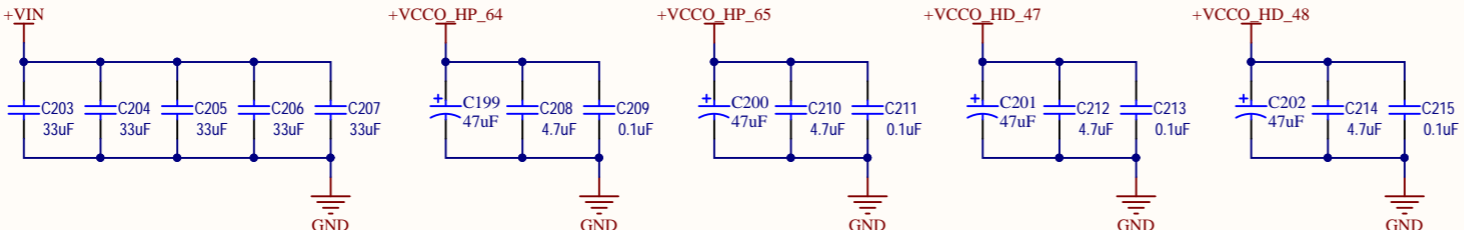
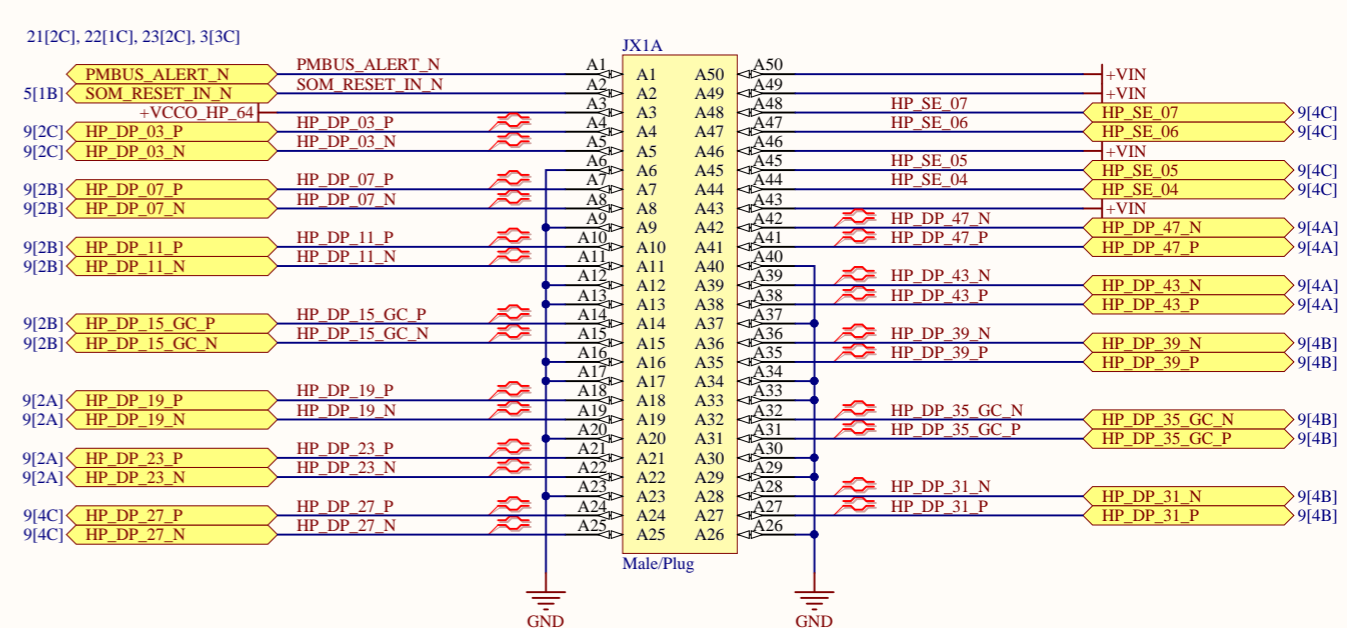
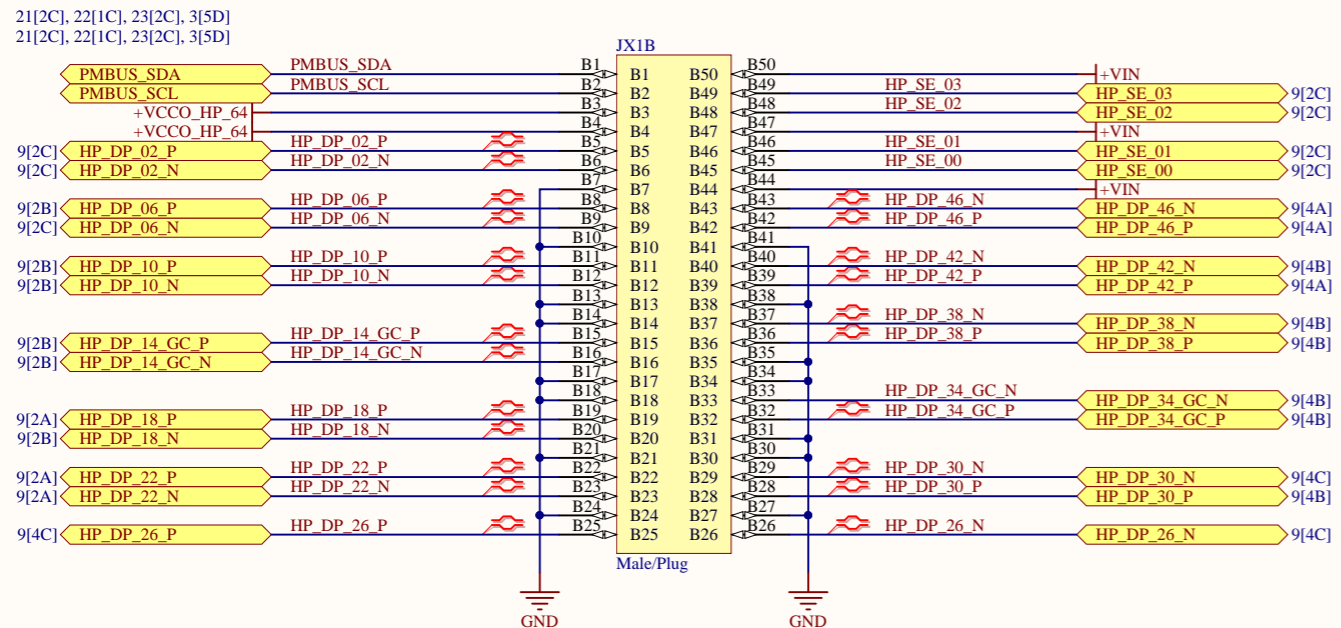
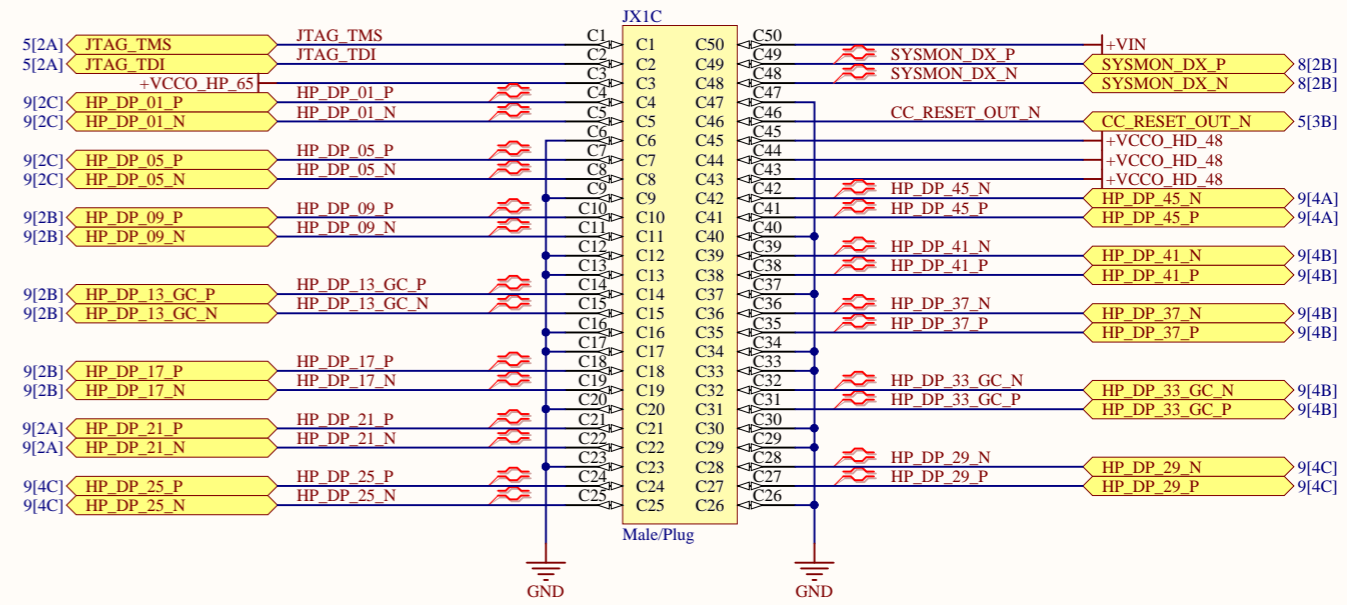
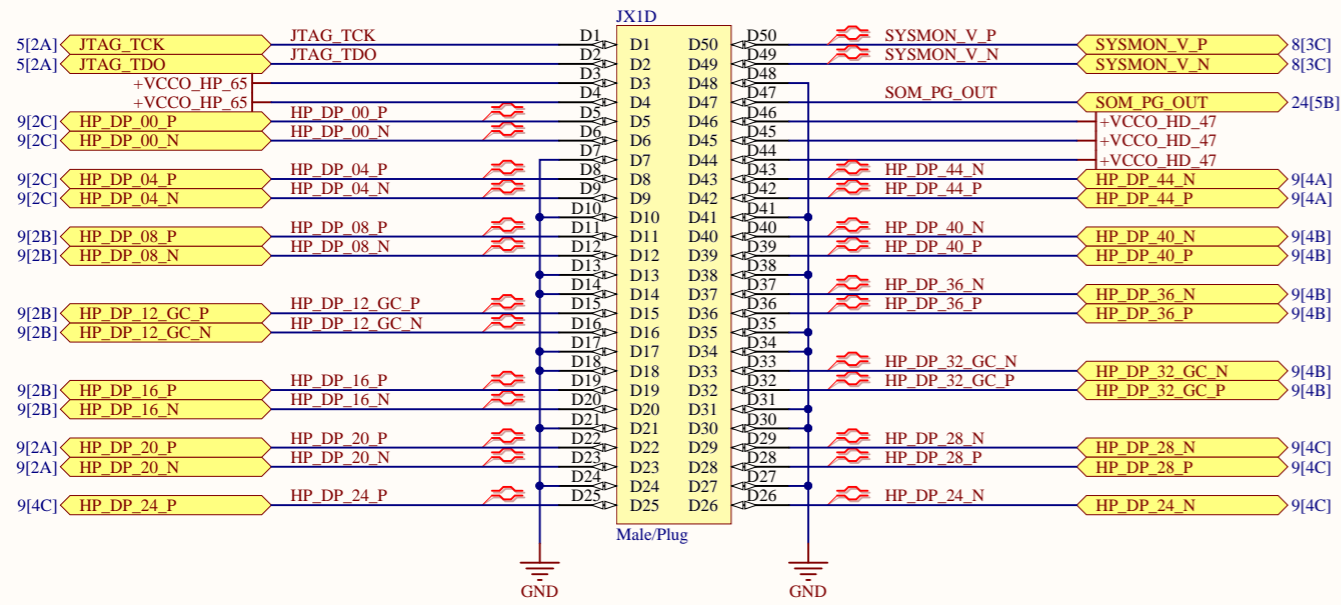


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NT1_PS_DDR_A14	NT2_PS_DDR_A14	NT2_PS_DDR_A14	15[1C]
NT1_PS_DDR_A15	NT2_PS_DDR_A15	NT2_PS_DDR_A15	15[1C]
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NT1_PS_DDR_BA1	NT2_PS_DDR_BA1	NT2_PS_DDR_BA1	15[1C]
NT1_PS_DDR_ACT_N	NT2_PS_DDR_ACT_N	NT2_PS_DDR_ACT_N	15[1C]
NT1_PS_DDR_PARITY	NT2_PS_DDR_PARITY	NT2_PS_DDR_PARITY	15[1C]
NT1_PS_DDR_CS0_N	NT2_PS_DDR_CS0_N	NT2_PS_DDR_CS0_N	15[1C]
NT1_PS_DDR_BG0	NT2_PS_DDR_BG0	NT2_PS_DDR_BG0	15[1C]
NT1_PS_DDR_ODT0	NT2_PS_DDR_ODT0	NT2_PS_DDR_ODT0	15[1C]
NT1_PS_DDR_CKE0	NT2_PS_DDR_CKE0	NT2_PS_DDR_CKE0	15[1C]
NT1_PS_DDR_RAM_RST_N	NT2_PS_DDR_RAM_RST_N	NT2_PS_DDR_RAM_RST_N	15[1C]
NT1_PS_DDR_ALERT_N	NT2_PS_DDR_ALERT_N	NT2_PS_DDR_ALERT_N	15[1C]
NT1_PS_DDR_CK0_P	NT2_PS_DDR_CK0_P	NT2_PS_DDR_CK0_P	15[1C]
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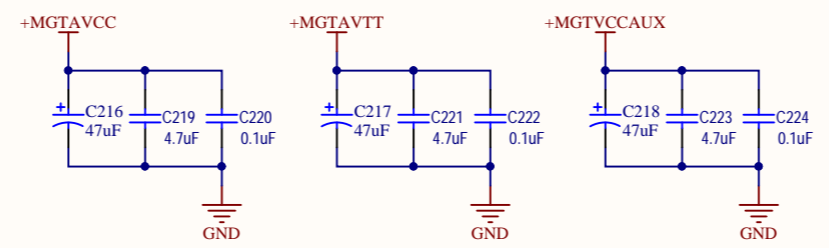
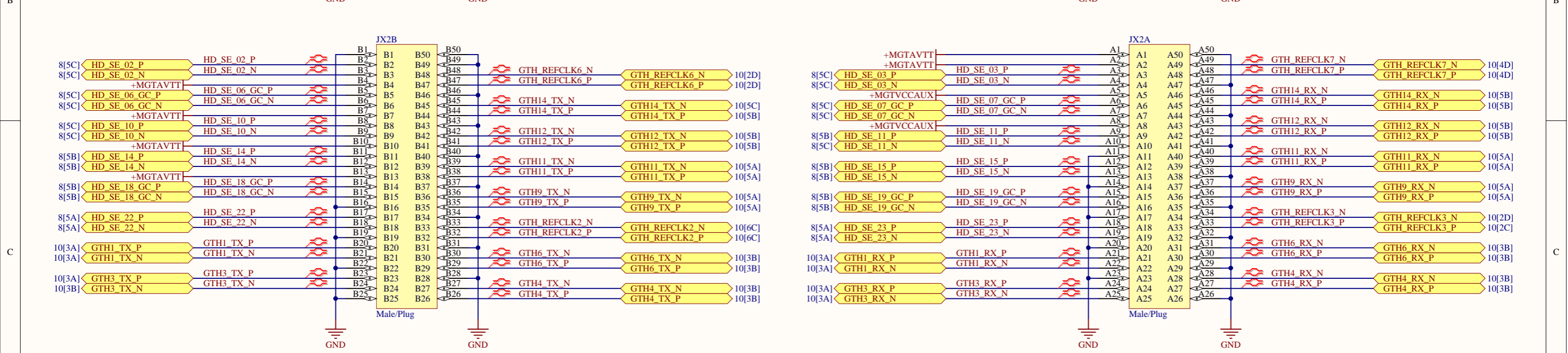
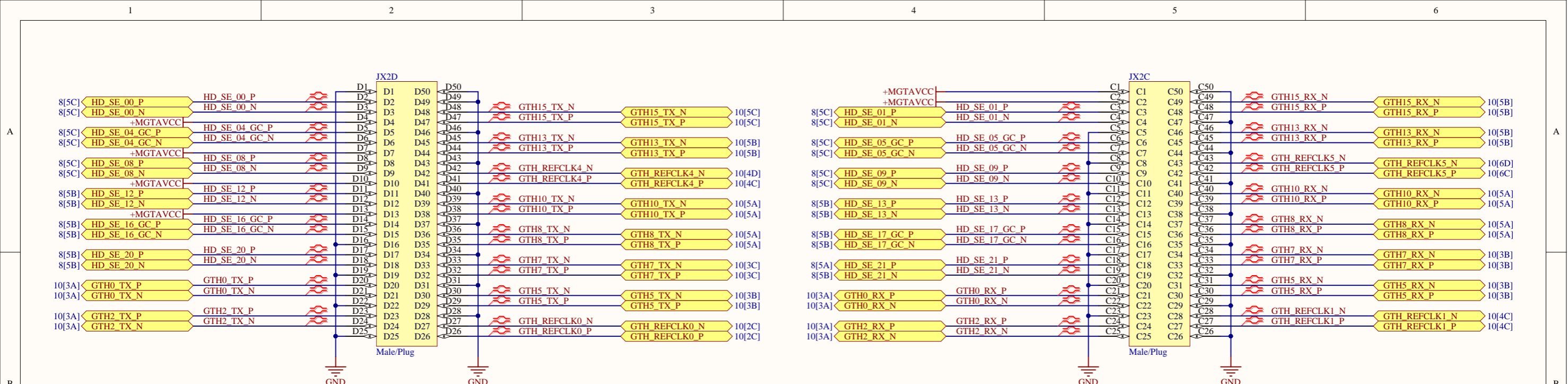




DESIGN NOTE: Use ONLY +16V or better capacitors on +VIN for 12V support.

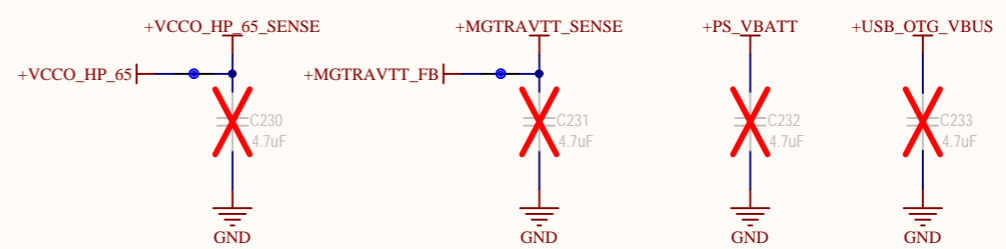
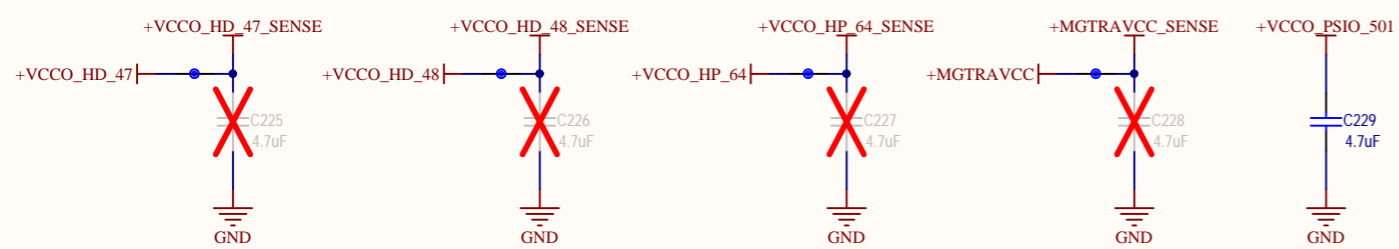
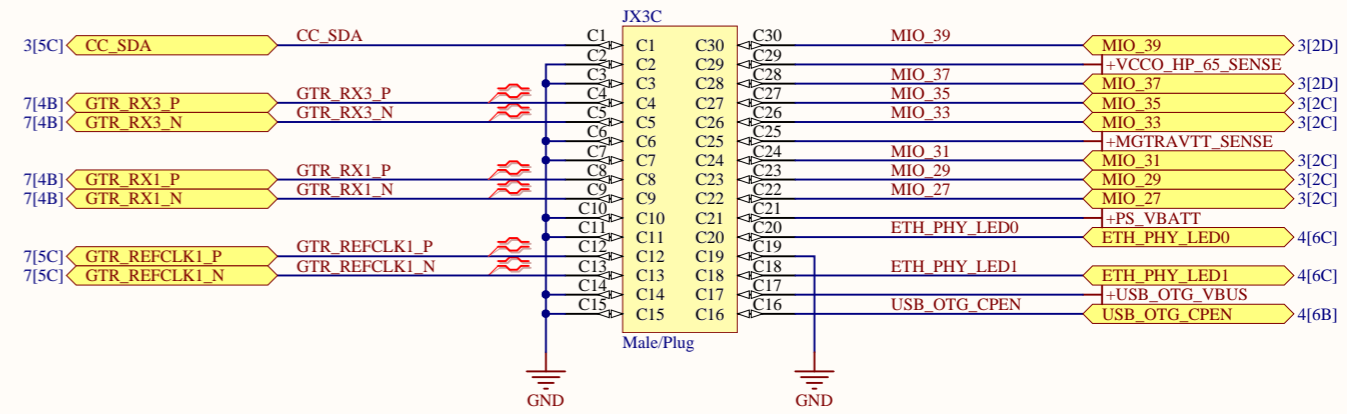
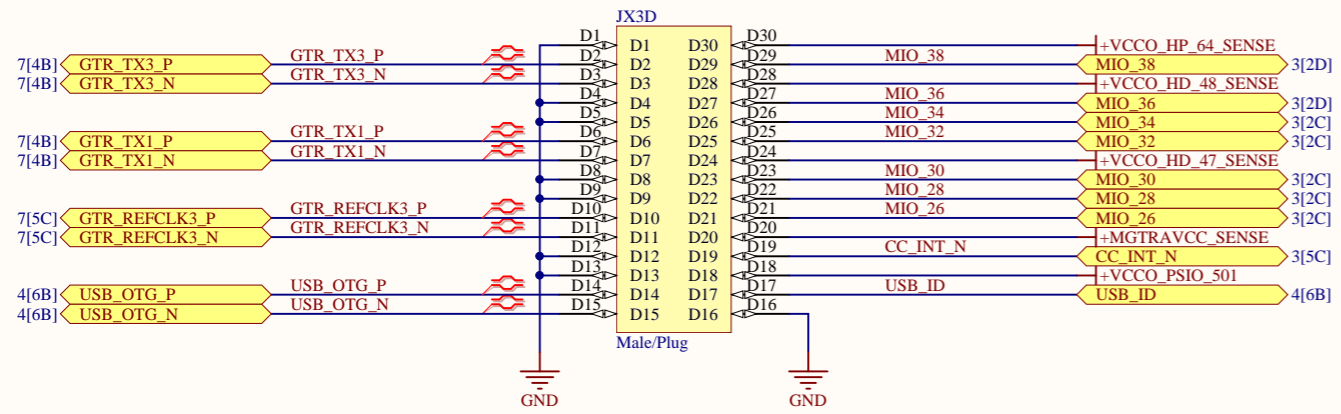
AVNET Avnet Engineering Services

Project Name:	UltraZed-EV SOM	PCB Rev:	BOM:	Variant:
Doc Num:	SCH-US2SOM	1	01	03
Sheet Title:	18 - JX1 Micro Header.SchDoc	Date:	2/1/2018	Time: 4:00:32 PM
Size:	B	Sheet:	18 of 25	

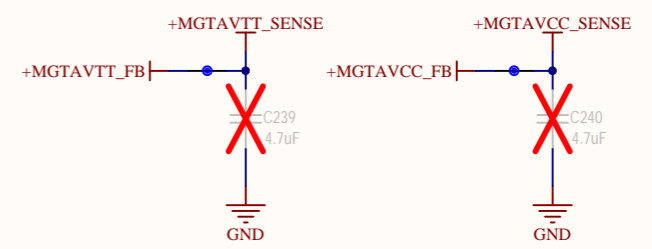
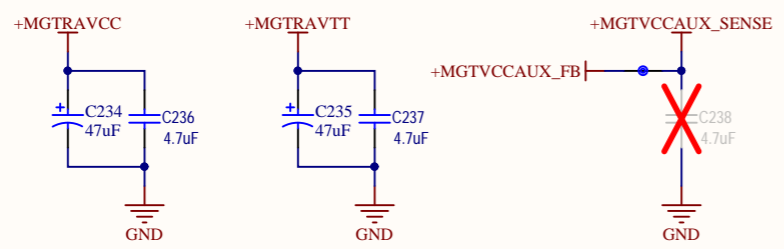
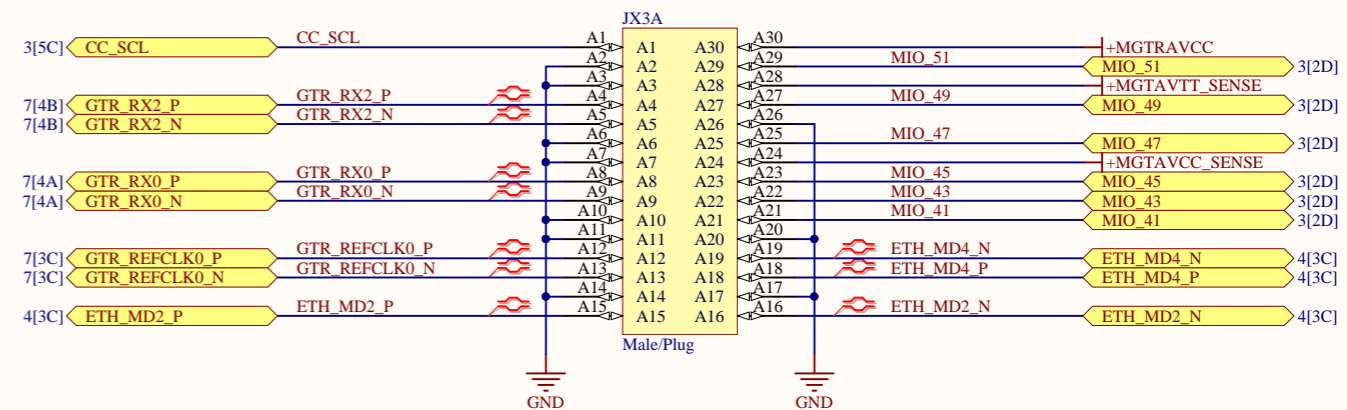
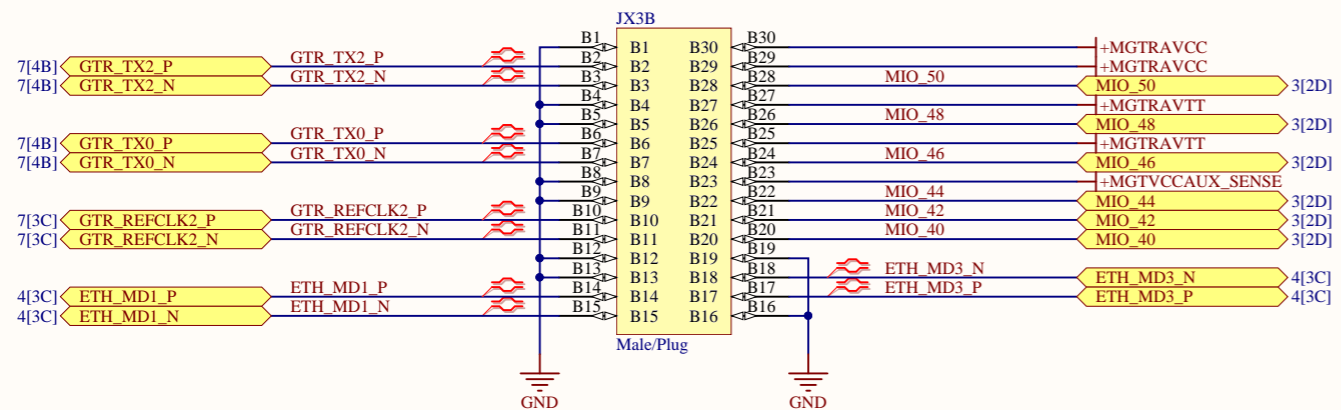


AVNET Avnet Engineering Services

Project Name:	UltraZed-EV SOM	PCB Rev:	BOM:	Variant:
Doc Num:	SCH-US2SOM	Date:	2/1/2018	Time:
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				19 of 25

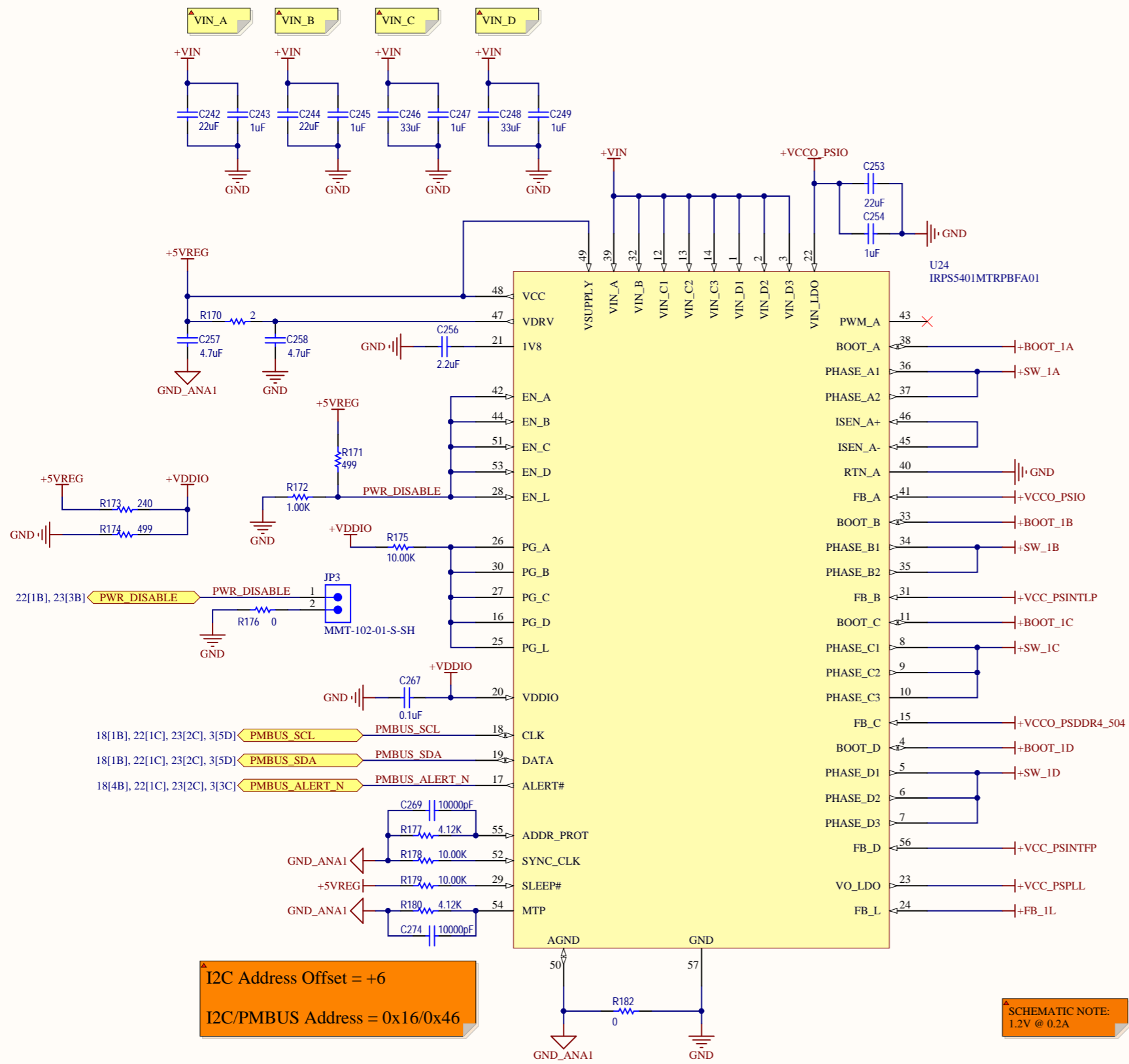


DESIGN NOTE: Use ONLY +10V or better capacitors on +VBUS for 5V support.
DNP so as to not affect USB OTG Operation.

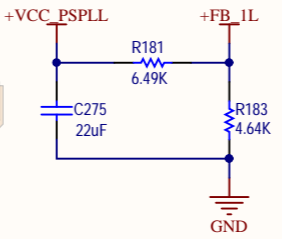
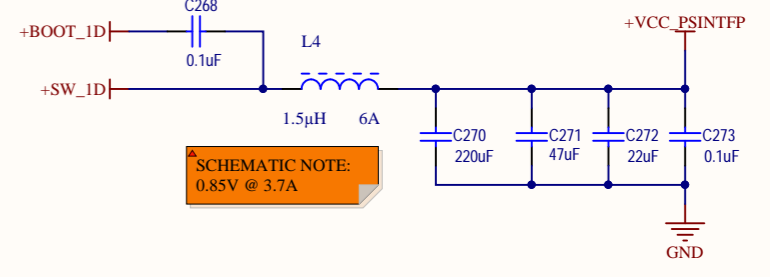
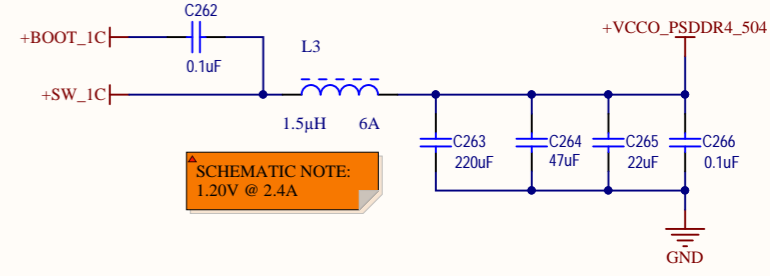
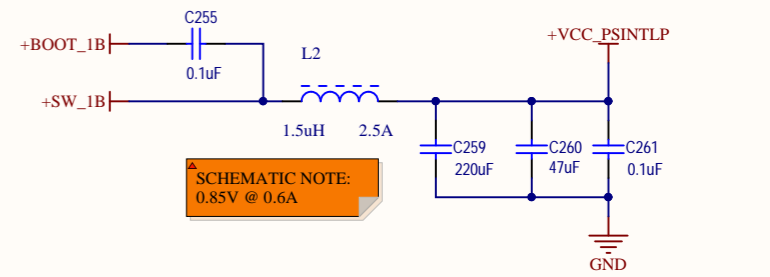
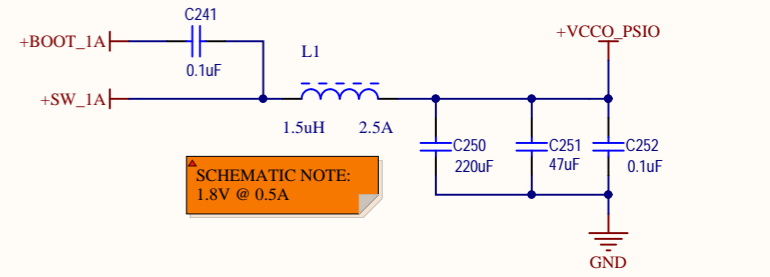


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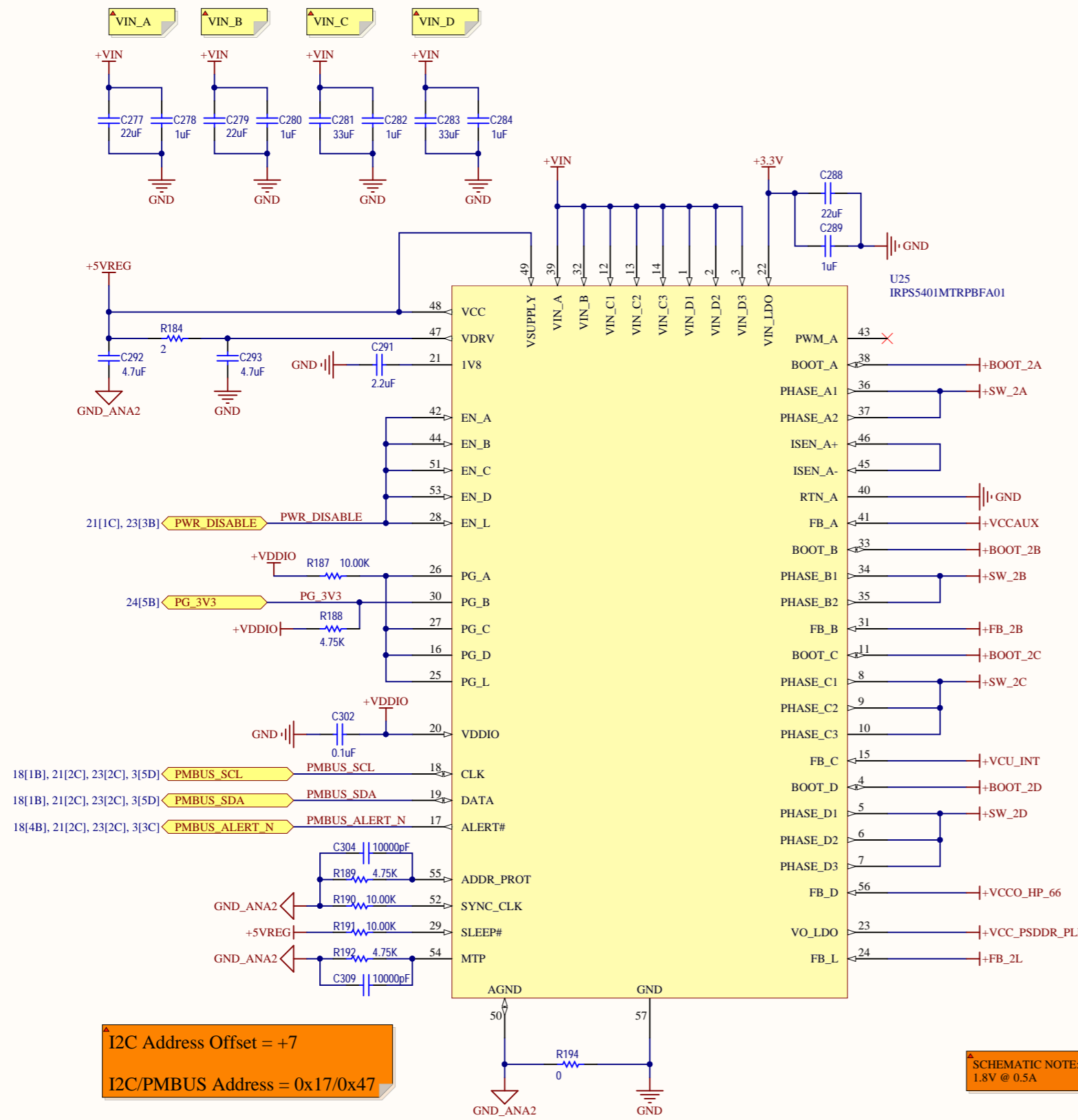
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Sheet:	B	Size:	20 of 25	Sheet:



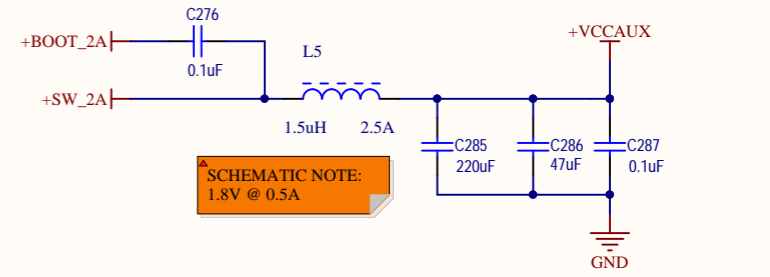
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I2C/PMBUS Address = 0x16/0x46



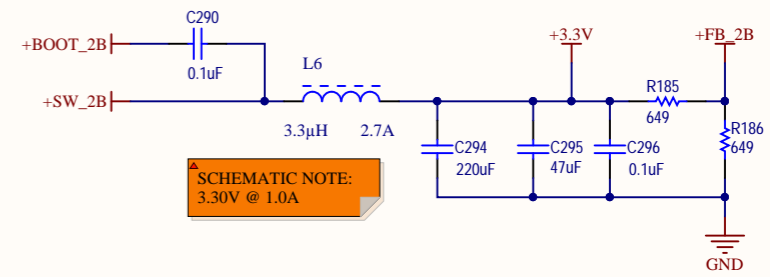
SCHEMATIC NOTE:
1.2V @ 0.2A



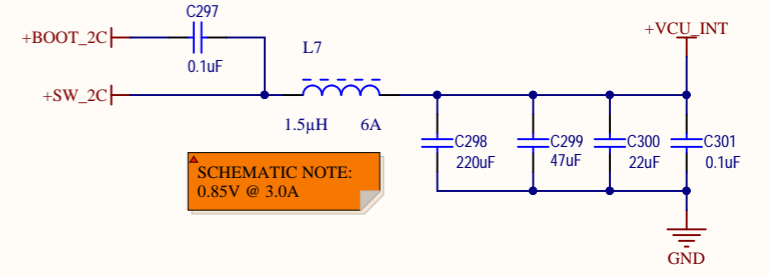
I2C Address Offset = +7
 I2C/PMBUS Address = 0x17/0x47



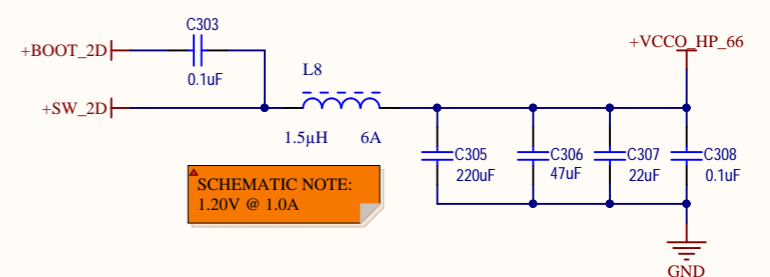
SCHEMATIC NOTE:
1.8V @ 0.5A



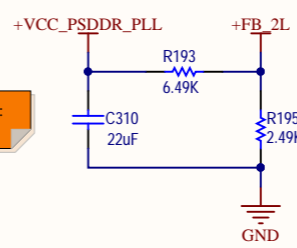
SCHEMATIC NOTE:
3.30V @ 1.0A



SCHEMATIC NOTE:
0.85V @ 3.0A

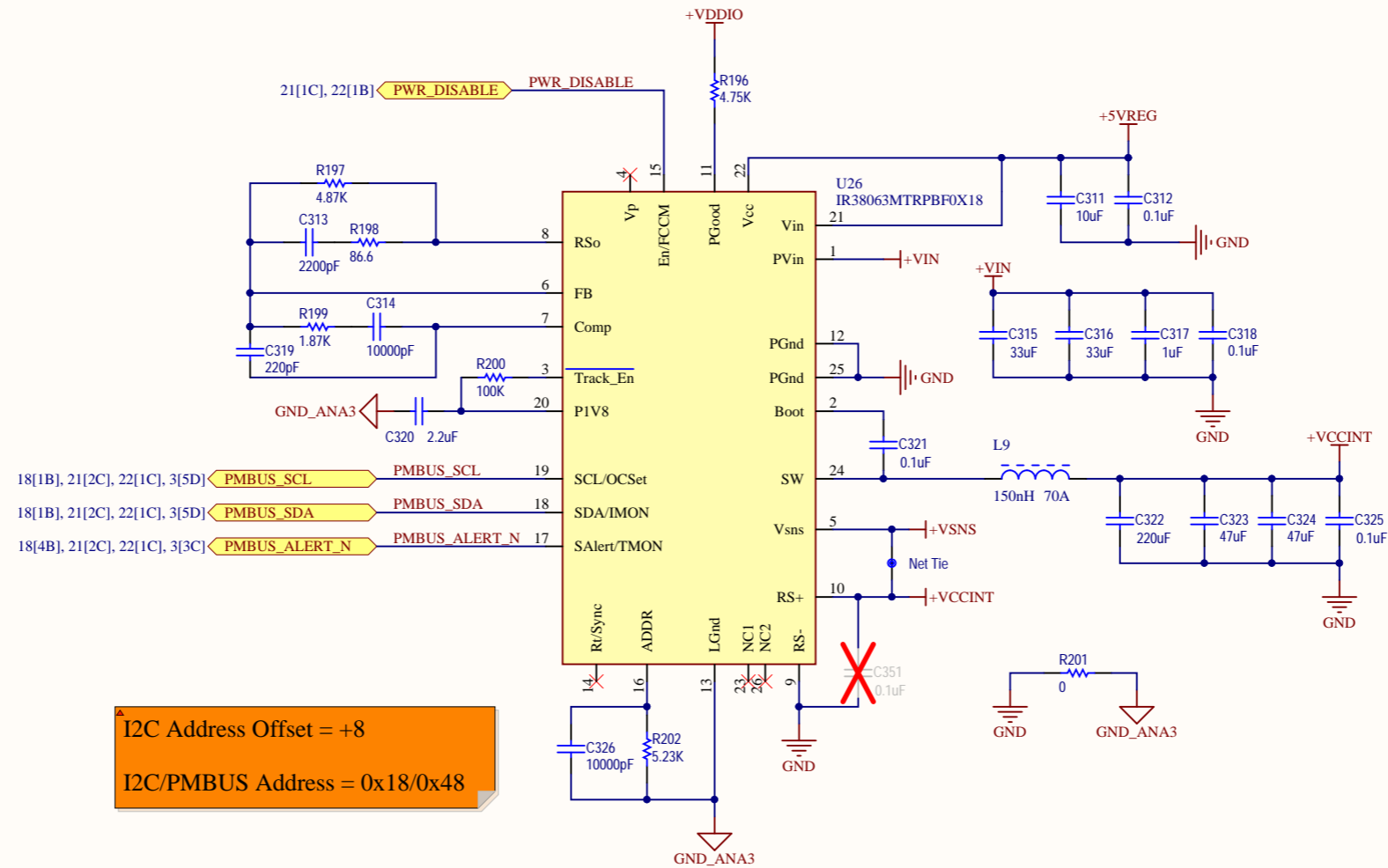


SCHEMATIC NOTE:
1.20V @ 1.0A

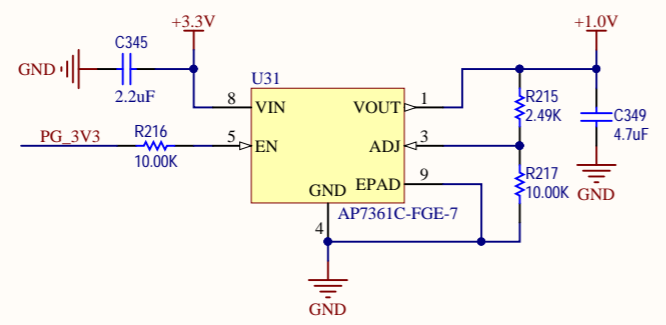
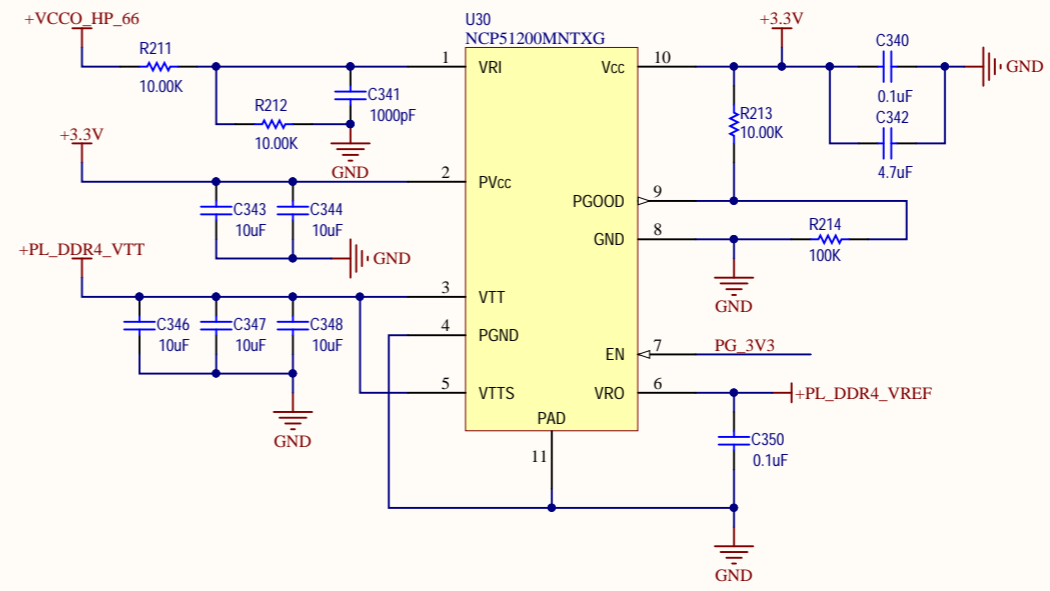
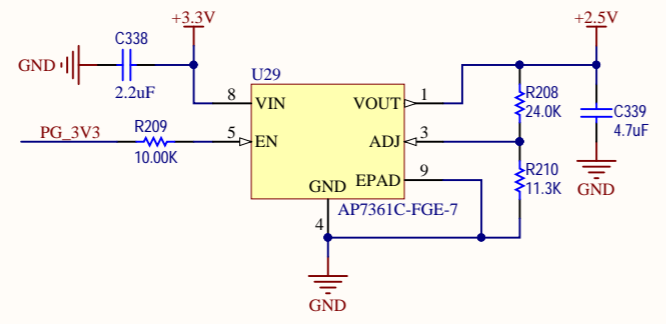
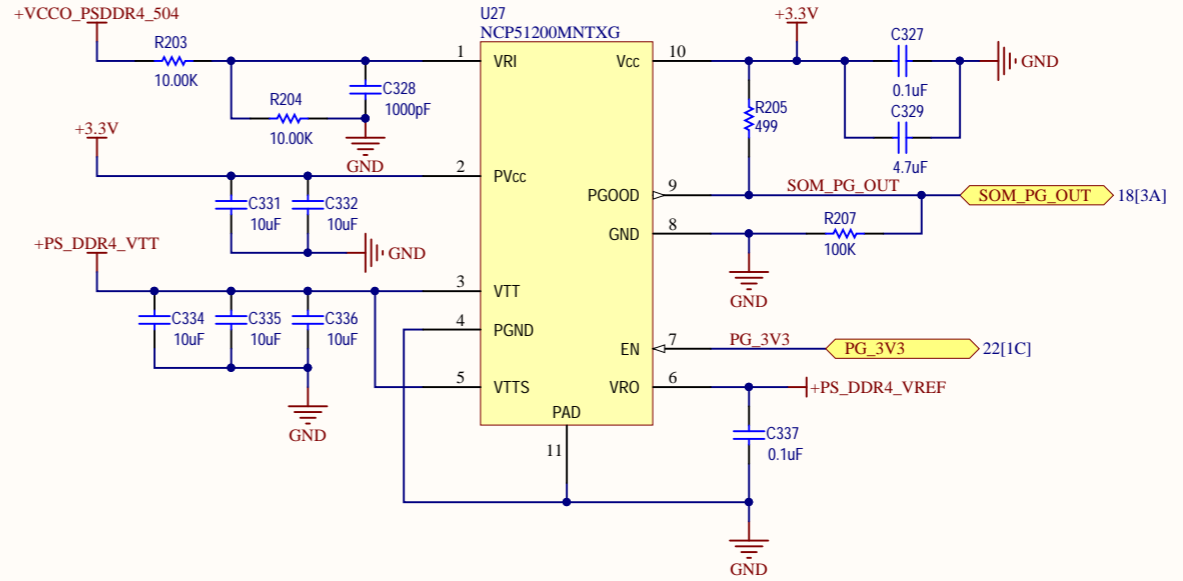
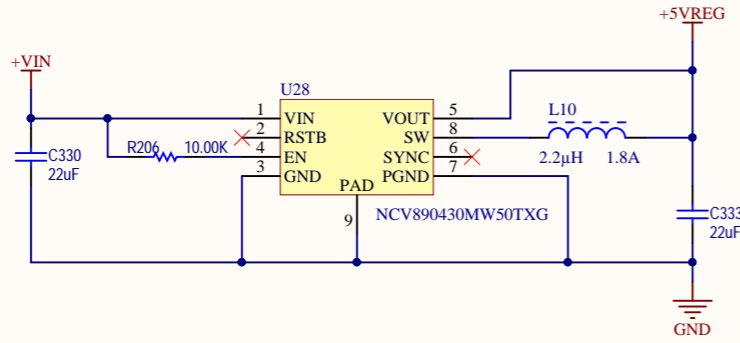


SCHEMATIC NOTE:
1.8V @ 0.5A

AVNET Avnet Engineering Services			
Project Name:	UltraZed-EV SOM	PCB Rev:	BOM: 01
Doc Num:	SCH-US2SOM	Date:	2/1/2018
Sheet Title:	22 - PMIC Power Supply #2.SchDoc	Time:	4:00:36 PM
Size:	B	Sheet:	22 of 25




I2C Address Offset = +8
 I2C/PMBUS Address = 0x18/0x48



Assembly:

Label1
BD-XXXX-XXXX-G
Label, Product

Label2

XXXXXXX
Label, Serial Number

ESD1

ESD Bag

Label_ESD1

Label, ESD

SS1

Trash Can-Silk Screen

SS2

RoHS 2-Silk Screen

Mechanicals:


PCB

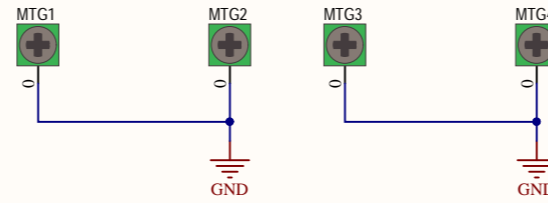
XXX-XXX-PCB-X
PCB PN (In Copper)

MECH1

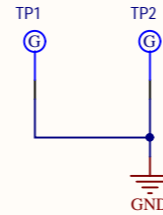
Plastic Frame Clip

NOTE: 31mm Heatsink
Frame Clip for U1
Utilize MaxiGRIP Tool PN
#MGT310 for Installation

Mounting Holes:



GND Test Points:



Jumper Shunts:

SH1

2SN-BK-G

SH2

2SN-BK-G

AVNET Avnet Engineering Services			
Project Name:	UltraZed-EV SOM	PCB Rev:	1
Doc Num:	SCH-US2SOM	BOM:	01
Sheet Title:	25 - Back Page.SchDoc	Variant:	03
	Date:	2/1/2018	Time:
			4:00:37 PM
	Size:	B	Sheet:
			25 of 25