SLG4G42480

GreenPAK ™

Interrupt Controller

General Description

Dialog SLG4G42480 is a low power and small form device. The SoC is housed in a 2mm x 2.2mm STQFN package which is optimal for using with small devices.

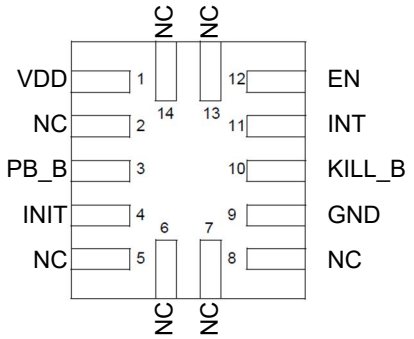
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Output Summary

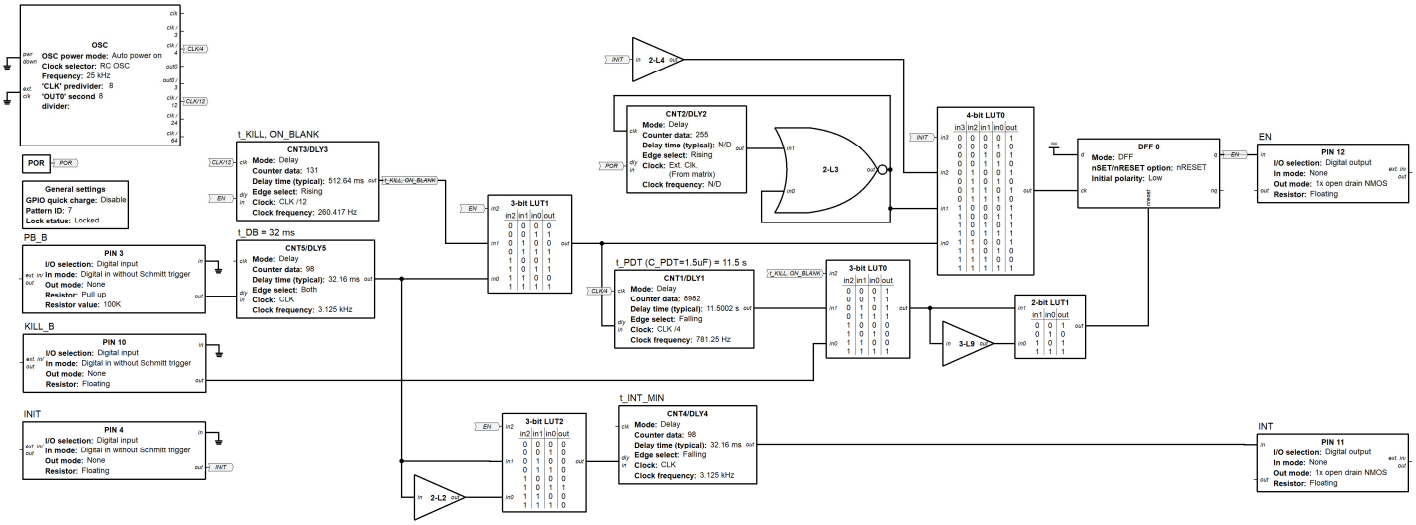
2 Outputs - Open Drain NMOS 1X

Pin Configuration



14-pin STQFN
(Top View)

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	PB_B	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
4	INIT	Digital Input	Digital Input without Schmitt trigger	floating
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	NC	--	Keep Floating or Connect to GND	--
8	NC	--	Keep Floating or Connect to GND	--
9	GND	GND	Ground	--
10	KILL_B	Digital Input	Digital Input without Schmitt trigger	floating
11	INT	Digital Output	Open Drain NMOS 1X	floating
12	EN	Digital Output	Open Drain NMOS 1X	floating
13	NC	--	Keep Floating or Connect to GND	--
14	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG4G42480V	14-pin STQFN
SLG4G42480VTR	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	OD 1x	--	8	mA
Current at Input Pin		-1.0	1.0	mA
Input Leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

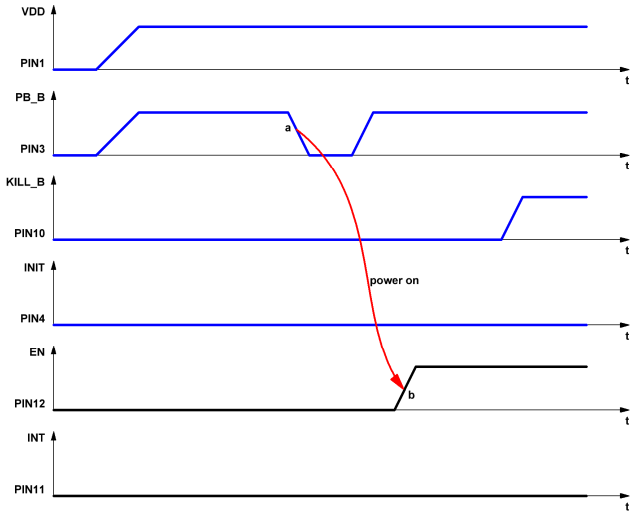
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PIN10 and PIN4 are LOW	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	1.780	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	--	--	1.210	V
V_{OL}	LOW-Level Output Voltage	Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	0.080	0.147	V
I_{OL}	LOW-Level Output Current (Note 1)	Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	7.313	12.370	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 3	70	100	130	kΩ
T_{DLY1}	Delay1 Time	At temperature 25°C	11.19	11.50	11.83	s
		At temperature -40 +85°C (Note 3)	10.06	11.50	13.97	s
T_{DLY3}	Delay3 Time	At temperature 25°C	497.14	512.64	529.18	µs
		At temperature -40 +85°C (Note 3)	447.11	512.64	624.75	µs
T_{DLY4}	Delay4 Time	At temperature 25°C	31.14	32.16	33.26	µs
		At temperature -40 +85°C (Note 3)	28.01	32.16	39.27	µs
T_{DLY5}	Delay5 Time	At temperature 25°C	31.14	32.16	33.26	µs

		At temperature -40 +85°C (Note 3)	28.01	32.16	39.27	µs
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

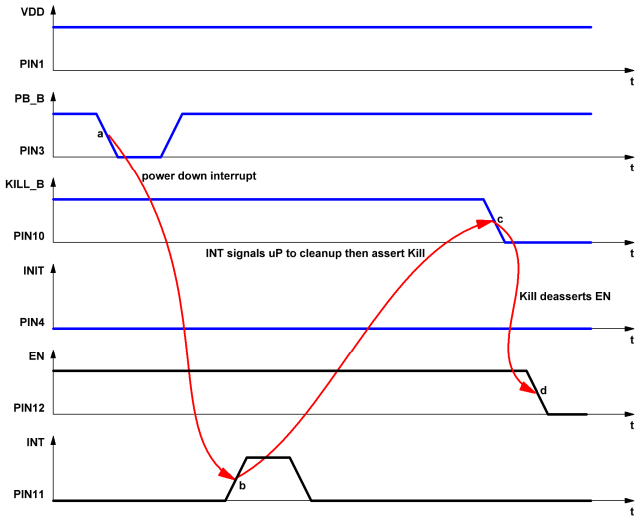
Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.
3. Guaranteed by Design.

Timing Diagram

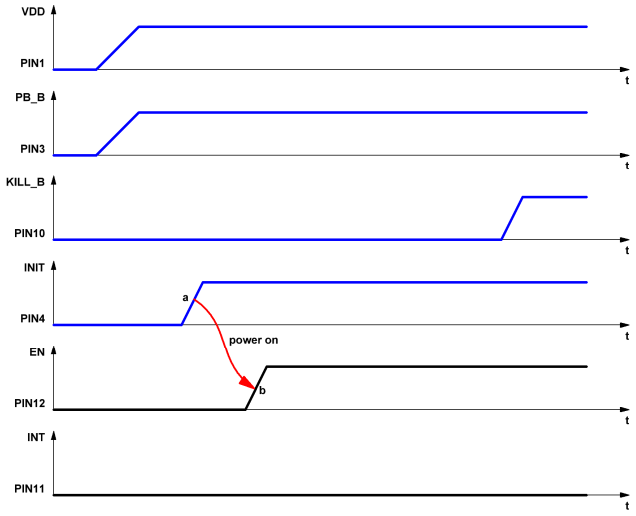
Power Up, INIT is Low, PB_B assert EN, Ignore Kill



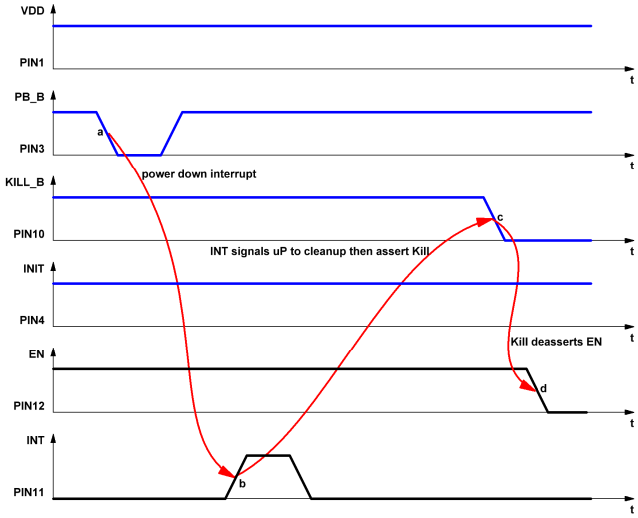
Power Down via Short Push, INIT is Low



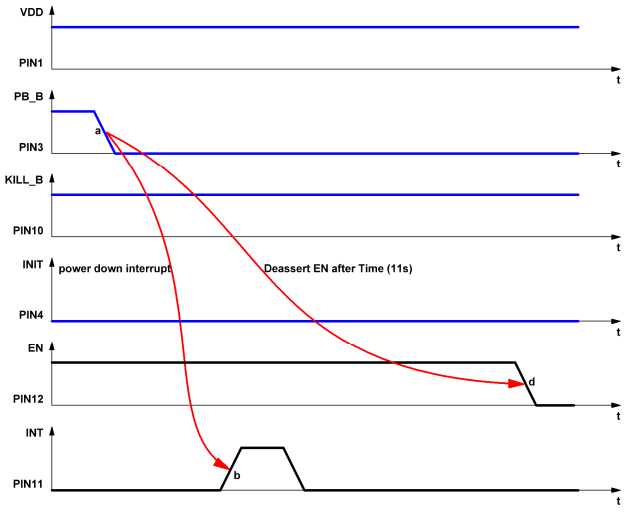
Power Up, INIT is High, Assert EN, Ignore Kill



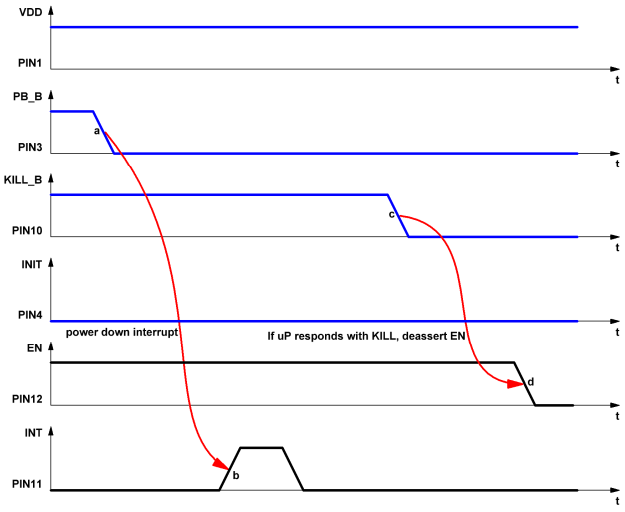
Power Down via Short Push, INIT is High



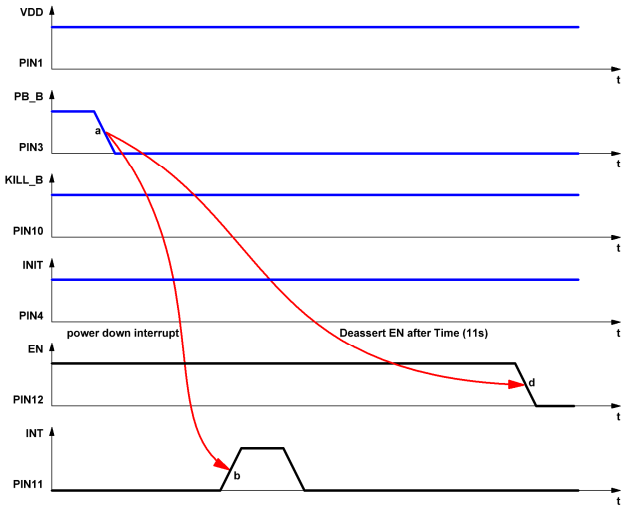
Power Down via Long Push, INIT is Low, No Kill



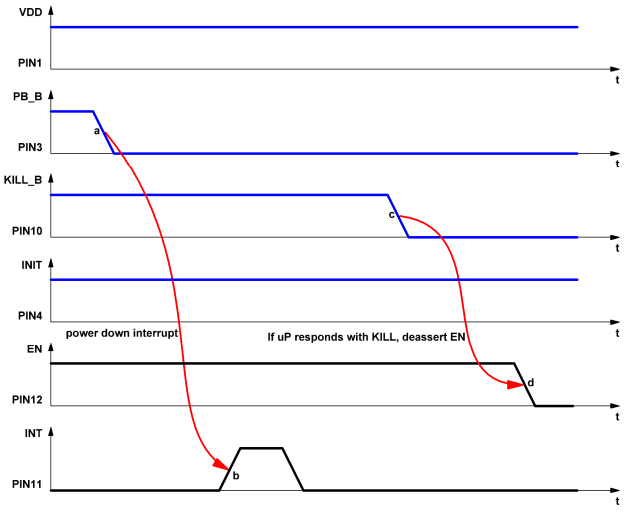
Power Down via Long Push, INIT is Low, Kill deasserts EN



Power Down via Long Push, INIT is High, No Kill



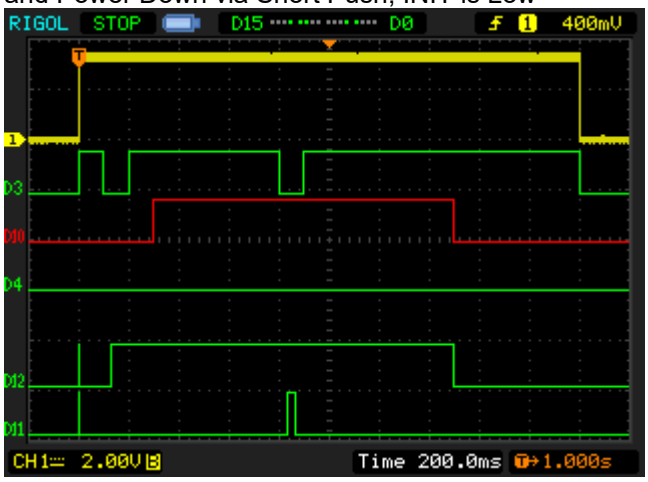
Power Down via Long Push, INIT is High, Kill deasserts EN



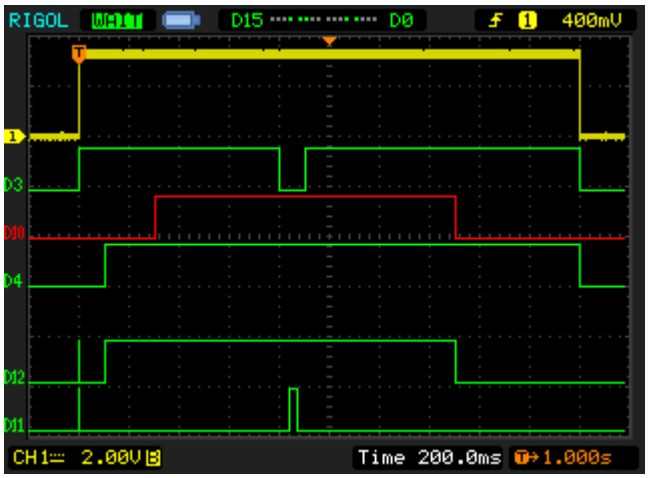
Functionality Waveforms

Channel 1 (yellow/top line) – PIN# 1 (VDD)
D3 – PIN#3 (PB_B)
D4 – PIN#4 (INIT)
D10 – PIN#10 (KILL_B)
D11 – PIN#11 (INT) with external 5kΩ pull up resistor
D12 – PIN#12 (EN) with external 5kΩ pull up resistor

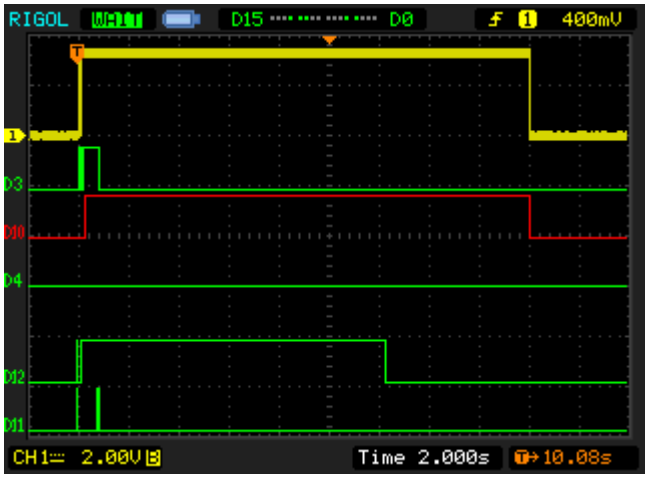
1. Power Up, INIT is Low, PB_B assert EN, Ignore Kill and Power Down via Short Push, INIT is Low



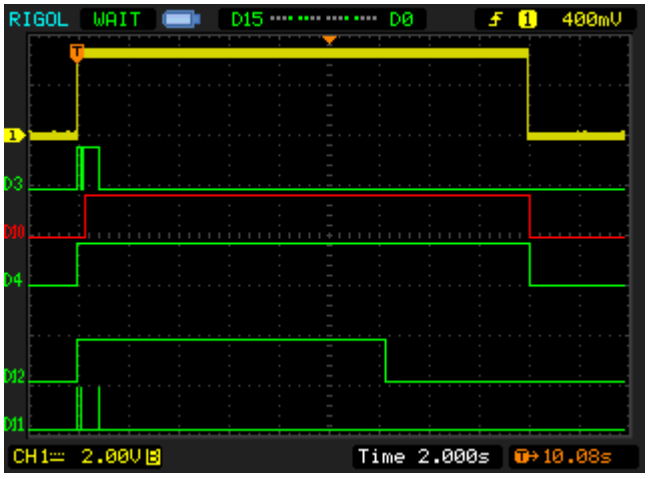
2. Power Up, INIT is High, Assert EN, Ignore Kill and Power Down via Short Push, INIT is High



3. Power Up, INIT is Low, PB_B assert EN, Ignore Kill and Power Down via Long Push, INIT is low, No Kill

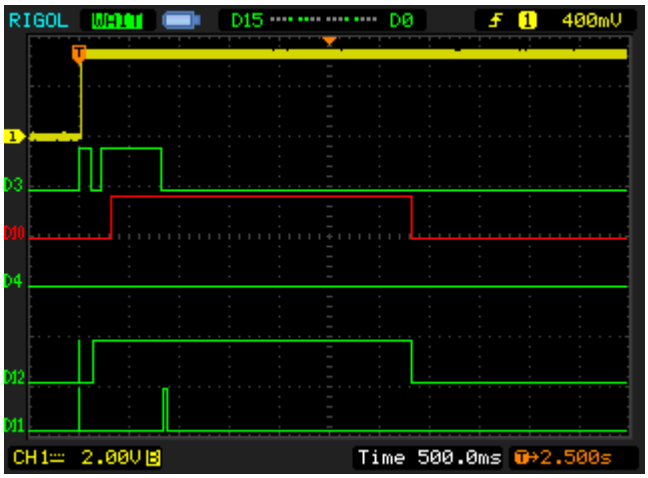


4. Power Up, INIT is High, Assert EN, Ignore Kill and Power Down via Long Push, INIT is high, No Kill

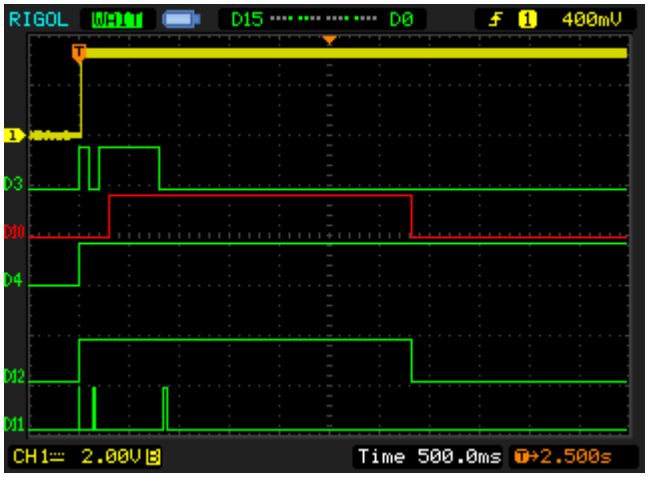


Channel 1 (yellow/top line) – PIN# 1 (VDD)
D3 – PIN#3 (PB_B)
D4 – PIN#4 (INIT)
D10 – PIN#10 (KILL_B)
D11 – PIN#11 (INT) with external 5kΩ pull up resistor
D12 – PIN#12 (EN) with external 5kΩ pull up resistor

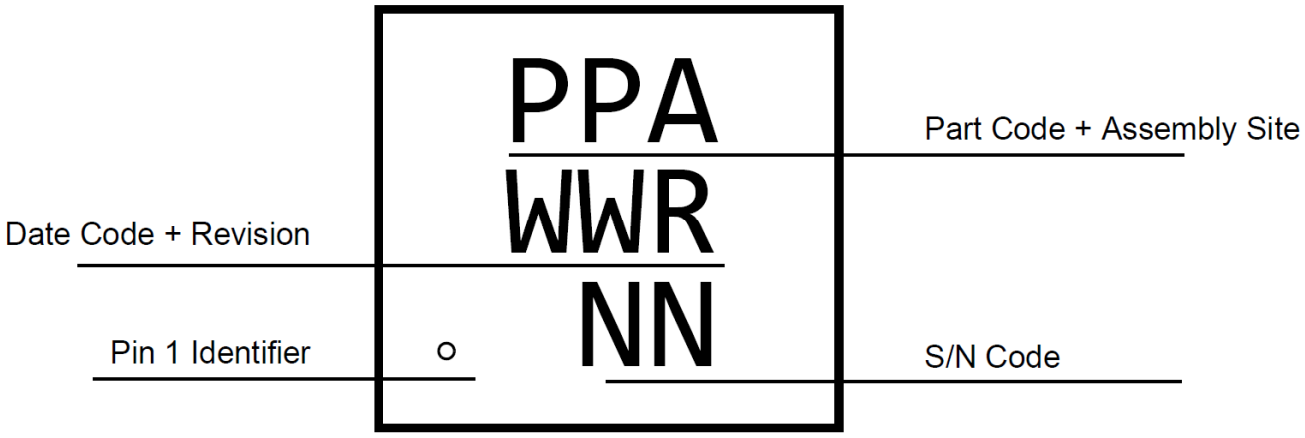
5. Power Up, INIT is Low, PB_B assert EN, Ignore Kill and Power Down via Long Push, INIT is low, Kill deasserts EN



6. Power Up, INIT is High, Assert EN, Ignore Kill and Power Down via Long Push, INIT is high, Kill deasserts EN



Package Top Marking

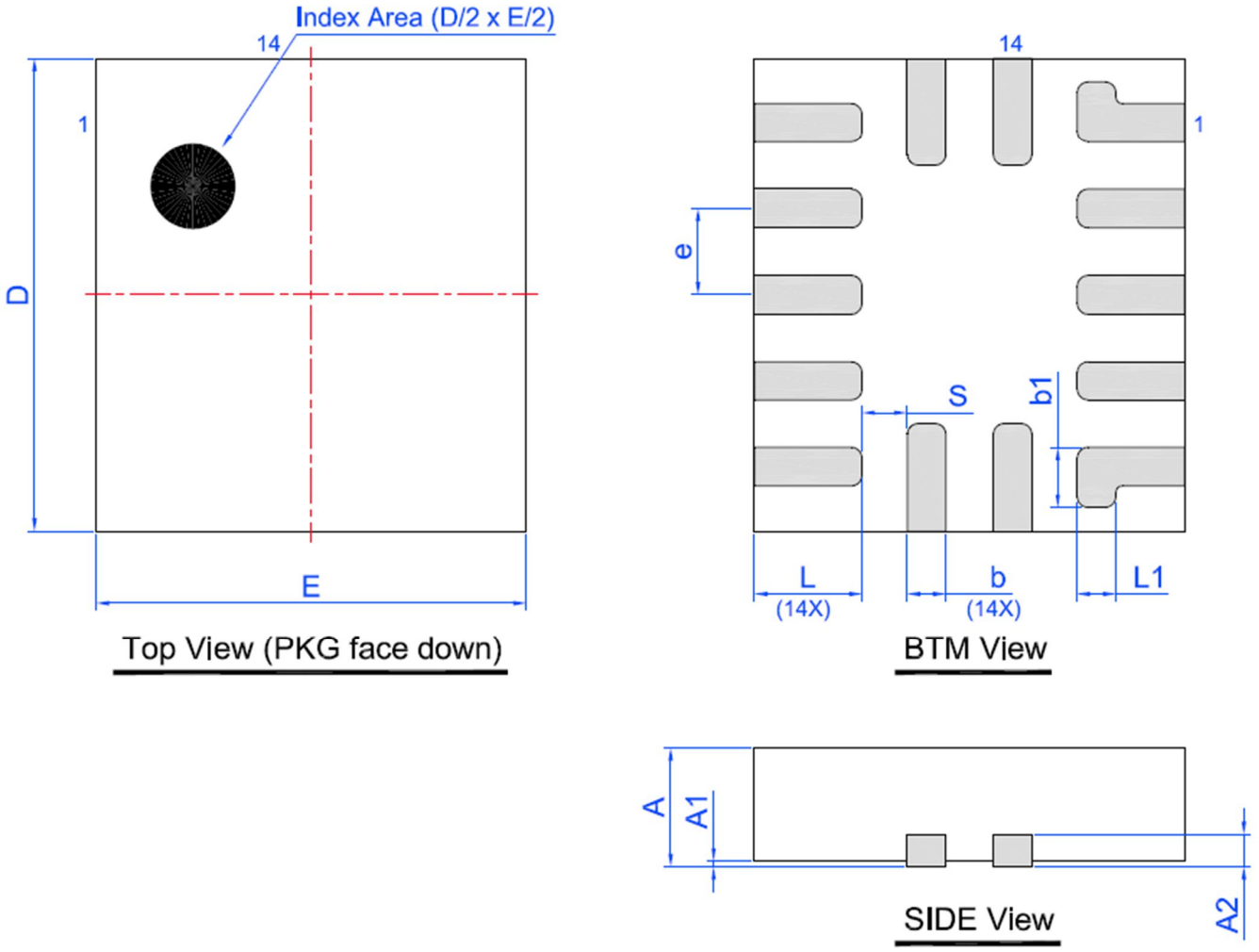


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	007	L	0x38C0C0BD	A5	E	04/25/2019

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

STQFN 14L 2 x 2.2mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

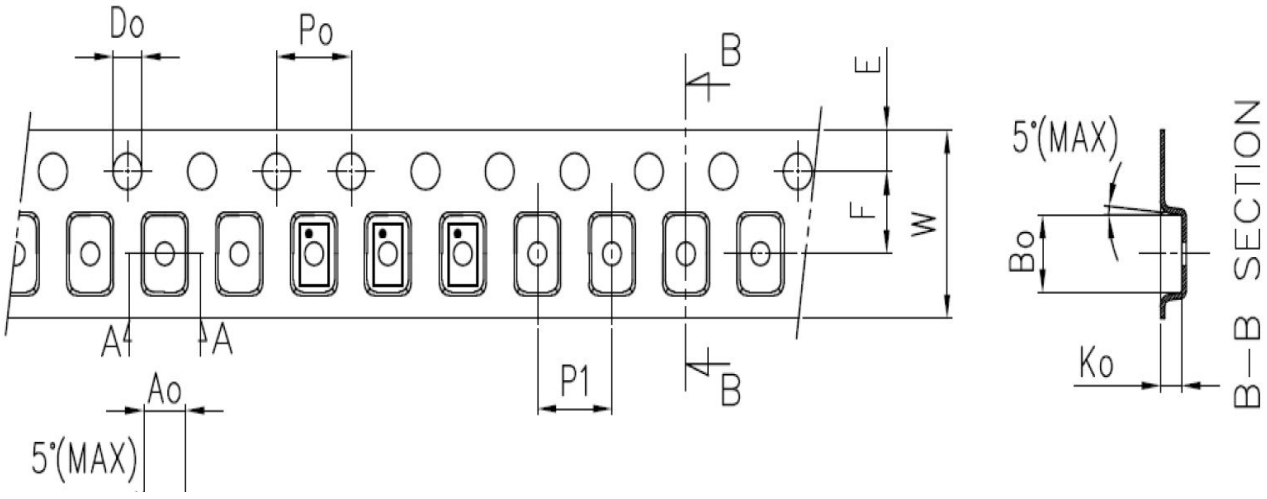
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.15	2.20	2.25
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.45	0.50	0.55
b	0.13	0.18	0.23	S	0.21 TYP		
e	0.40 BSC			b1	0.28 TYP		
				L1	0.18 TYP		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 2x2.2mm 0.4P COL	14	2x2.2x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

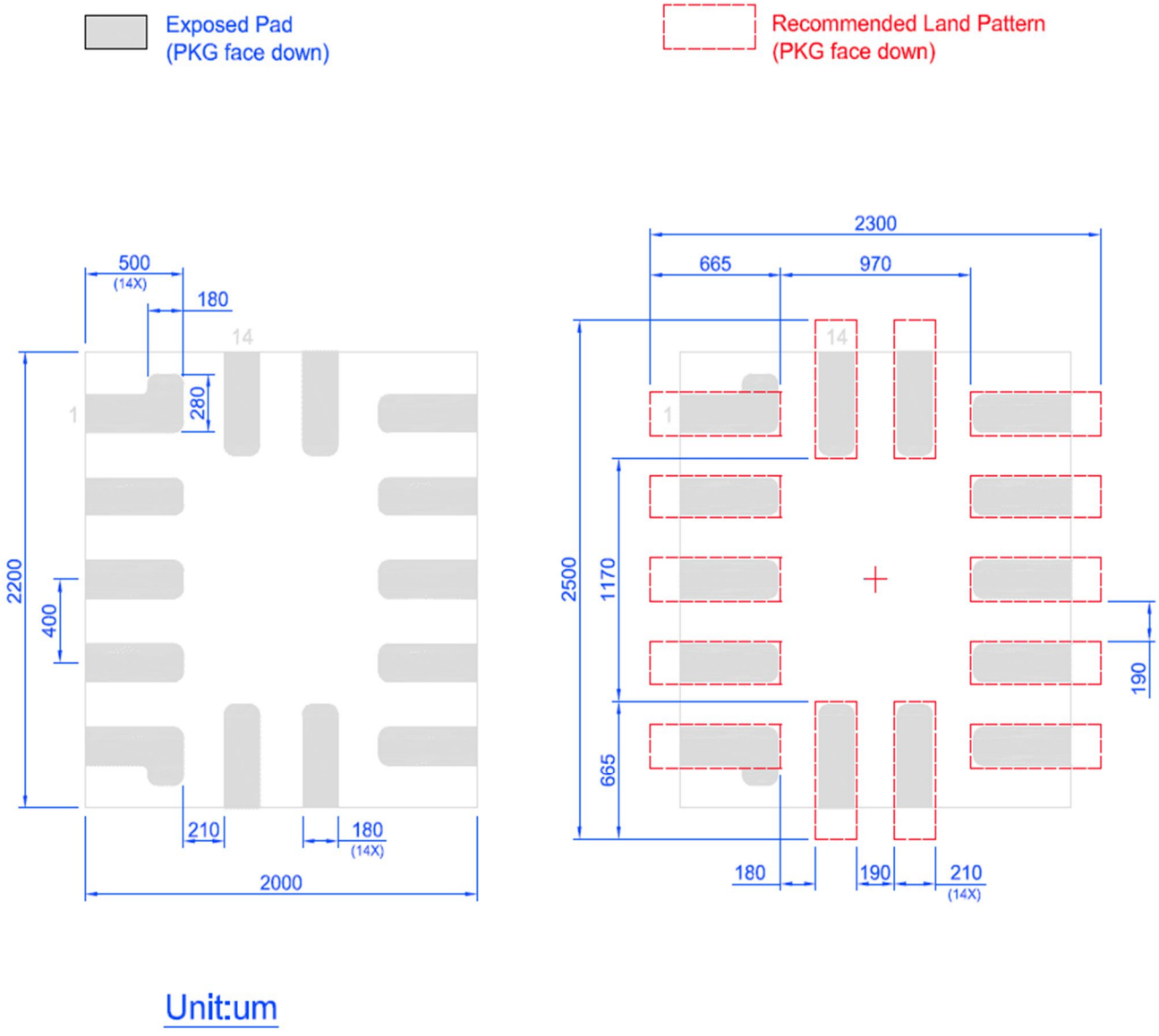
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 2x2.2 mm 0.4P COL	2.2	2.35	0.8	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.42 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



Unit:um

Datasheet Revision History

Date	Version	Change
05/08/2018	0.10	New design for SLG46170 chip
05/25/2018	0.11	Implemented invariable INTERRUPT period. Added ON_BLANK functionality to correct KILL_B work
05/30/2018	0.12	Updated Device Revision Table
06/27/2018	0.13	Added INIT-pin to select start-up logic
06/29/2018	0.14	Updated Device Revision Table
07/02/2018	0.15	Changed the name of PIN 11 (INT_B to INT)
07/18/2018	0.16	Corrected INIT-functionality
07/20/2018	0.17	Updated Device Revision Table
08/08/2018	0.18	Corrected functionality of KILL_B
08/08/2018	0.19	Updated Device Revision Table
11/20/2018	0.20	Fixed the issue of the INIT-function
04/15/2019	0.21	Updated Lock-Status
04/25/2019	1.00	Production Release

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