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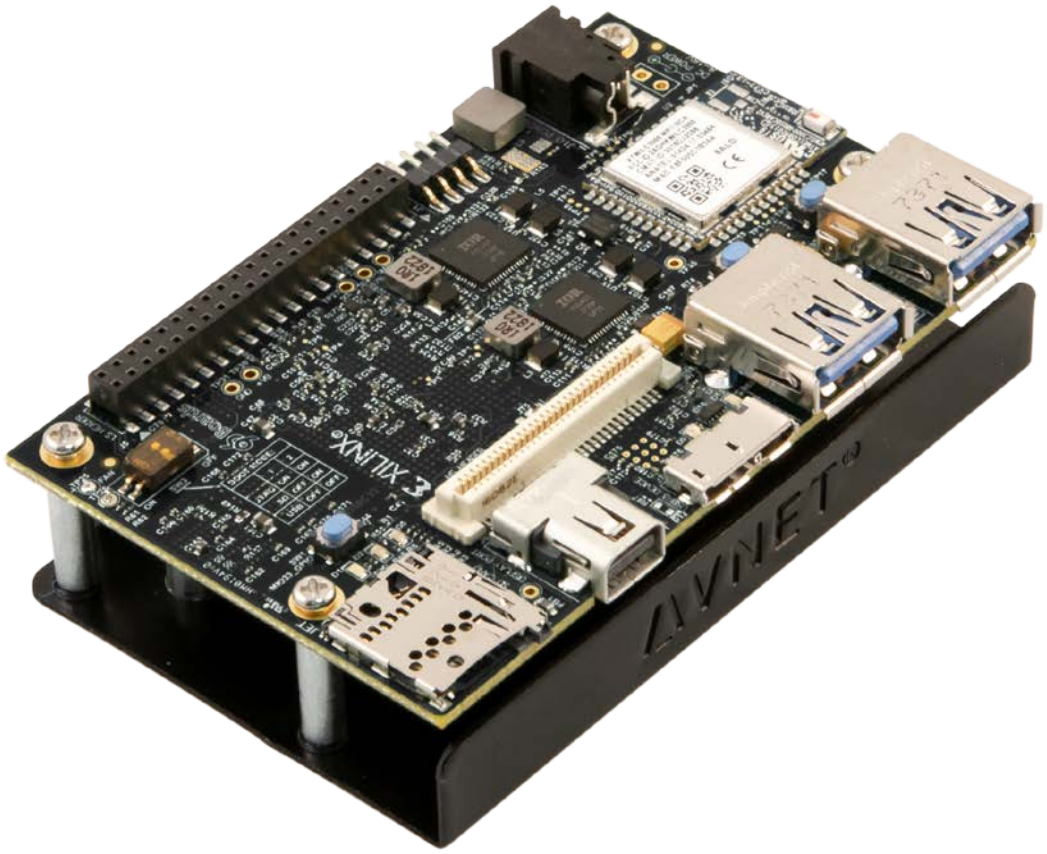

Ultra96-V2 Single Board Computer Hardware User's Guide

Version 1.3

LIT# Ultra96-V2-HW-User-Guide-v1.3

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1 Document Control

Document Version: 1.3

Document Date: 02 Jun 2021

2 Version History

Version	Date	Comment
1.0	07 Aug 2018	Initial Release
1.1	10 Nov 2020	Update to include information about I-grade and updated heatsink. Adding improved pin location tables. Removed I/O section from ZU+ section since I/Os are described throughout the document.
1.2	03 May 2021	Correcting Table references for Mezzanine tables. Corrected signal names for high-speed mezzanine.
1.3	02 Jun 2021	Corrected Bank 26 voltage in Programmable Logic section; Corrected Expansion identification and Bank 26 voltage in Table 7.

3 Introduction

The Ultra96-V2 is a low-cost Single Board Computer (SBC) targeted for broad use in many applications:

- Provide a Xilinx entry in the 96Boards community
- Offer a low-cost, Xilinx-based SBC in both Commercial (0ºC to 60ºC) and Industrial (-40ºC to +85ºC) temperature grades for engineers to adopt in development, proof-of-concept, and production projects
- Combine ARM processing with programmable logic in a convenient and expandable board
- Showcase a wide range of potential peripherals and acceleration engines in the programmable logic that is not available from other 96Boards offerings
- Be a low-cost starter kit for Zynq UltraScale+ MPSoC developers
- Showcase hardware acceleration for software bottlenecks
- Allow expansion to a variety of sensors and peripherals through the 96Boards mezzanine connectors
- Target many applications for development, including:
    - Artificial Intelligence
    - Machine Learning
    - IoT/Cloud connectivity for add-on sensors
    - Embedded Computing
    - Robotics
    - Wireless design and demonstrations using Wi-Fi and Bluetooth

3.1 Glossary

Term	Definition
ZU+	Zynq UltraScale+
MPSoC	Multi-Processor System on Chip
PS	Zynq UltraScale+ MPSoC Processing System
PL	Zynq UltraScale+ MPSoC Programmable Logic
MIO	PS Multiplexed Input Output Pins
POR	Power On Reset
APU	Application Processing Unit
RPU	Real-time Processing Unit
GPU	Graphics Processing Unit
SYSMON	System Monitor
HD	High Density PL I/O Pins
HP	High Performance PL I/O Pins
PMBus	Power Management Bus
AI	Artificial Intelligence
ML	Machine Learning
IoT	Internet of Things
AR	Answer Record

3.2 Reference Documents

[1] Zynq UltraScale+ MPSoC Overview

[2] Zynq UltraScale+ MPSoC DC and AC Switching Characteristics

[3] Zynq UltraScale+ MPSoC Technical Reference Manual

[4] Zynq UltraScale+ MPSoC Packaging and Pinout Product Specification

[5] Zynq UltraScale+ MPSoC PCB Design Guide

[6] UltraScale Architecture SelectIO Resources

[7] SBVA484 Package File

[8] Xilinx Vivado Design Suite

[9] Xilinx Vitis Unified Software Platform

[10] 96Boards Specification

[11] Microchip USB3320 Hi-Speed USB 2.0 ULPI Transceiver

[12] Microchip USB5744 Smart Hub

[13] Microchip ATWILC3000 Wi-Fi/BT Module

[14] Micron LPDDR4 SDRAM datasheet

[15] Delkin Devices Utility Industrial MLC microSD

4 Ultra96-V2 Architecture and Features

This section summarizes the features of the single board computer, followed by functional descriptions of each circuit.

4.1 List of Features

The Ultra96-V2 Single Board Computer supports the following features:

- Linaro 96Boards Consumer Edition compatible
- Xilinx Zynq UltraScale+ MPSoC ZU3EG SBVA484
- Memory/storage
    - Micron 2 GB (512M x32) LPDDR4 Memory
    - MicroSD Socket
        - C-grade ships with Delkin Utility MLC 16GB card
        - I-grade ships with Delkin Utility+ Industrial-temperature MLC 16GB card
- Microchip Wi-Fi / Bluetooth
- Renesas (IDT) VersaClock 6E clock generator for LVDS and single-ended clocks
- Infineon and ON Semiconductor high efficiency power management
- Mini DisplayPort (MiniDP or mDP)
- 1x USB 3.0 Type Micro-B upstream port
- 2x USB 3.0 Type A downstream ports
- 1x USB 2.0 downstream port on high speed expansion
- 40-pin 96Boards Low-speed (LS) expansion header
- 60-pin 96Boards High speed (HS) expansion header
- Thermally dissipative device
    - Rev 1, datecodes 1935 and earlier: Mounted on thermal bracket with fan
    - Rev 1, datecodes 1936 and later: Custom Aavid passive heatsink
    - Rev 2 and later: Custom Aavid passive heatsink

Note that there is no on-board, wired Ethernet interface, although this can be added through the expansion connectors or USB. All communications without add-ons must be done via USB, Wi-Fi, JTAG, or expansion interface.

4.2 Ultra96-V2 Block Diagram

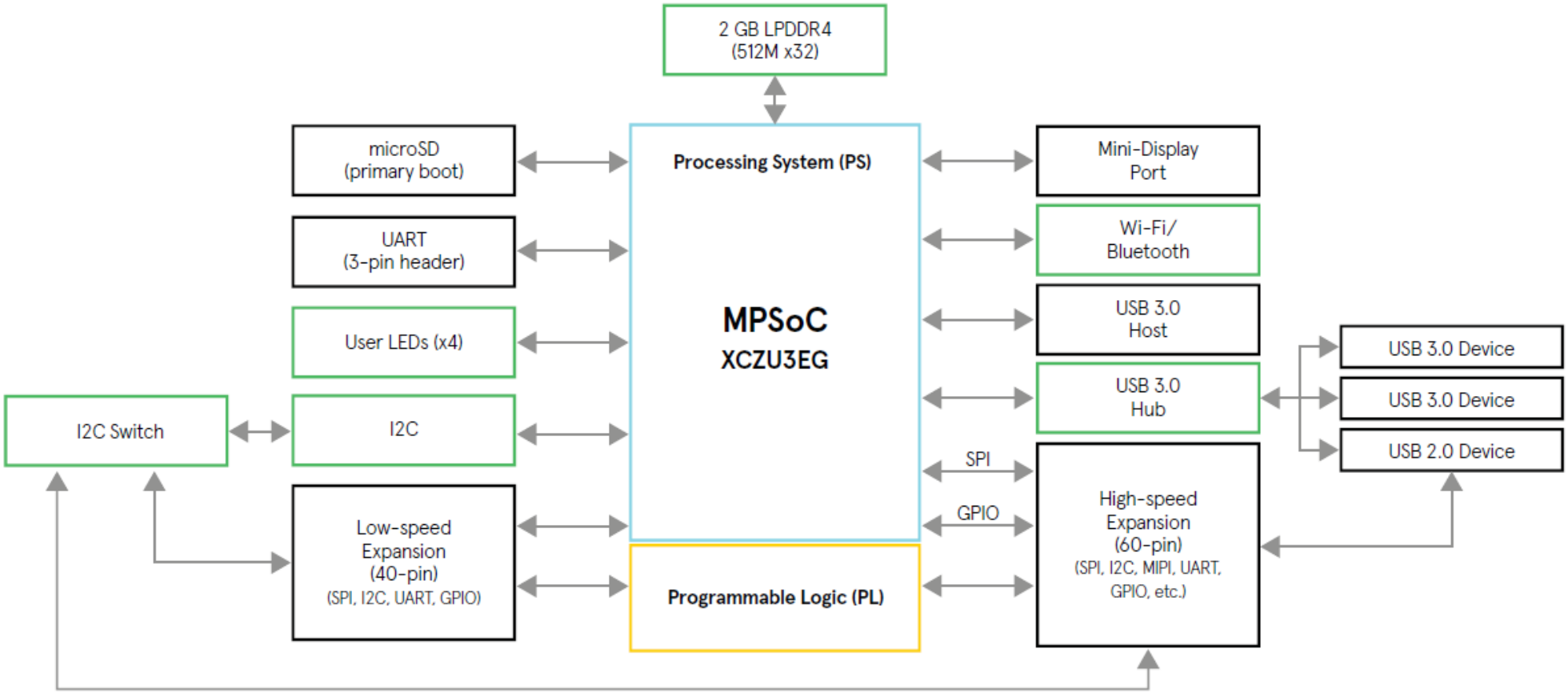


Figure 1 – Ultra96-V2 Block Diagram

5 Functional Description

The following sections provide brief descriptions of each feature provided on the Ultra96-V2 SBC.

5.1 Zynq UltraScale+ MPSoC

Ultra96-V2 features a Zynq UltraScale+ MPSoC ZU3EG device (in the SBVA484 package).

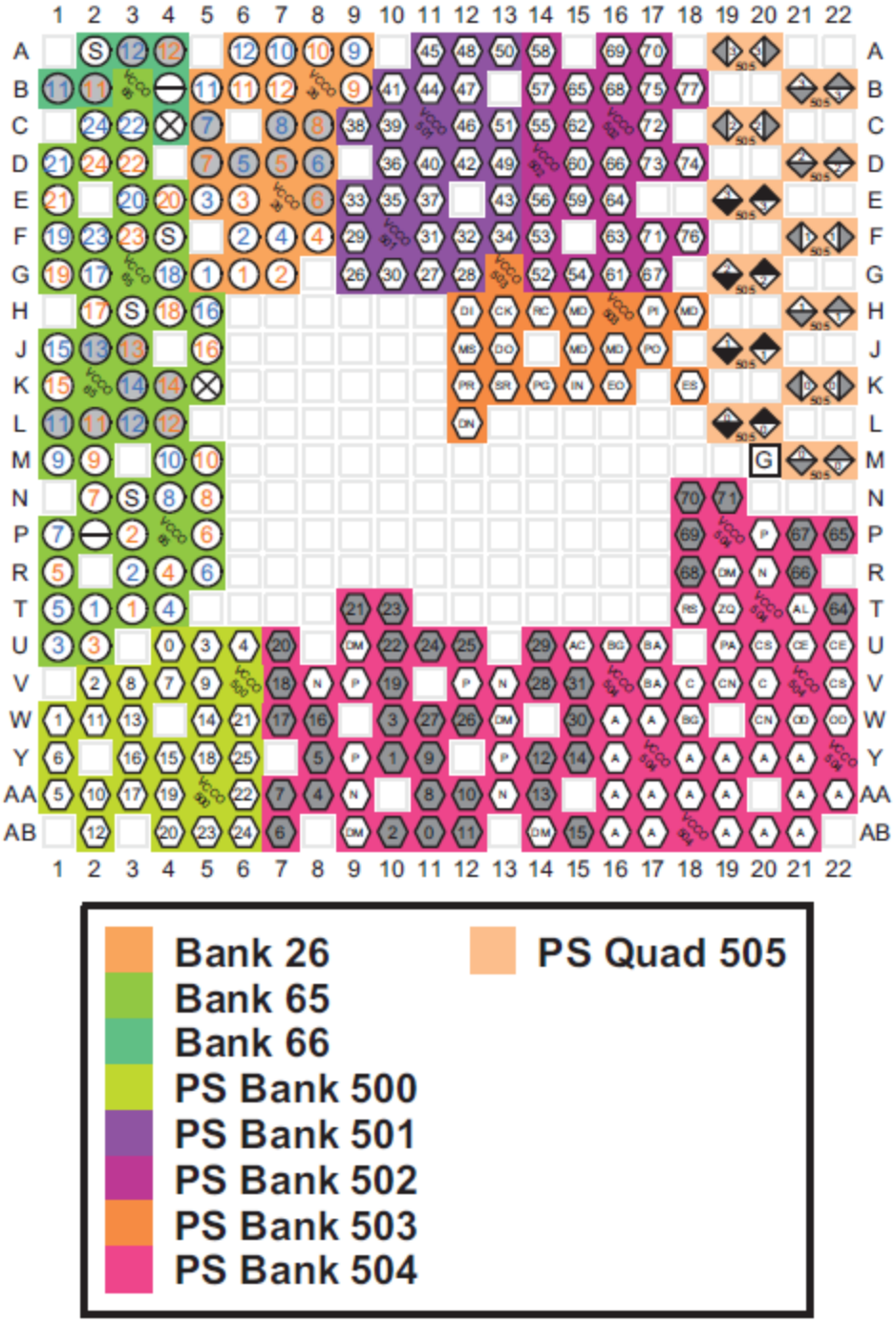


Figure 2 – SBVA484 Package Diagram

5.1.1 Processor System (PS)

- **Application Processing Unit**
  Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache
- **Real-Time Processing Unit**
  Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM
- **Embedded and External Memory**
  256KB On-Chip Memory w/ECC; External DDR memory controller (LPDDR4 on U96V2)
- **General Connectivity**
  214 PS I/O; UART; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters
- **High-Speed Connectivity**
  4 PS-GTR; DisplayPort 1.2a; USB 3.0
- **Graphic Processing Unit**
  ARM Mali™-400 MP2; 64KB L2 Cache

5.1.2 PS MIOs (Banks 500, 501, 502)

The Zynq UltraScale+ MPSoC Processing System (PS) provides 78 flexible multiplexed I/O (MIO) (configured as three banks of 26 I/Os) for peripheral pin assignment. These MIO support a wide variety of peripheral interfaces, with bank voltage support ranging from 1.8V to 3.3V.

The Ultra96-V2 connects all three MIO banks to 1.8V.

- VCCO_PSIO0_500 = +VCC_PSAUX = 1.8V
- VCCO_PSIO0_501 = +VCC_PSAUX = 1.8V
- VCCO_PSIO0_502 = +VCC_PSAUX = 1.8V

The default peripheral configuration for the three MIO banks is shown in the Vivado Block Design screenshots below. The descriptions and specific pinouts are shown in the three tables that follow.

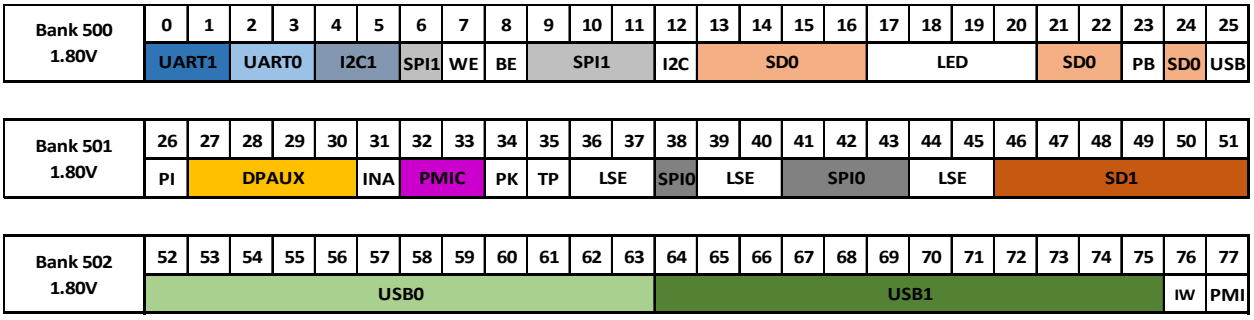


Figure 3 – MIO Default Peripheral Assignments on Ultra96-V2

Table 1 – PS MIO Bank 500 (1.8V, MIOs 0 to 25)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
AA2	PS_MIO10_500	MIO10_SPI1_MISO	96Boards High Speed Expansion Connector	J4	11
W2	PS_MIO11_500	MIO11_SPI1_MOSI		J4	1
Y1	PS_MIO6_500	MIO6_SPI1_SCLK		J4	9
V5	PS_MIO9_500	MIO9_SPI1_CS		J4	7
AB2	PS_MIO12_500	MIO12_I2C_MUX_RESET_N	I2C Port Expander	U7	24
U6	PS_MIO4_500	MIO4_I2C1_SCL		U7	19
AA1	PS_MIO5_500	MIO5_I2C1_SDA		U7	20
AB6	PS_MIO24_500	MIO24_SD0_DETECT	microSD Card Cage	J2	9
W3	PS_MIO13_500	MIO13_SD0_DAT0	microSD SDIO	U3	6
W5	PS_MIO14_500	MIO14_SD0_DAT1		U3	7
Y4	PS_MIO15_500	MIO15_SD0_DAT2		U3	1
Y3	PS_MIO16_500	MIO16_SD0_DAT3		U3	3
W6	PS_MIO21_500	MIO21_SD0_CMD		U3	4
AA6	PS_MIO22_500	MIO22_SD0_CLK		U3	9
AB5	PS_MIO23_500	MIO23_GPIO_PB	MIO23 Push Button	SW1	1
AA3	PS_MIO17_500	MIO17_PS_LED3	PS LEDs	Q5	5
Y5	PS_MIO18_500	MIO18_PS_LED2		Q5	2
AA4	PS_MIO19_500	MIO19_PS_LED1		Q3	5
AB4	PS_MIO20_500	MIO20_PS_LED0		Q3	2
V4	PS_MIO7_500	MIO7_RAD_RST_N	Radio Reset: MIO or PL Select	JT5	1
U4	PS_MIO0_500	MIO0_UART1_TX	UART Level Translator to Pod Connector	Q2	2
W1	PS_MIO1_500	MIO1_UART1_RX		Q1	2
Y6	PS_MIO25_500	MIO25_VBUS_DET	VBUS Detect Level Translator	Q14	2
V2	PS_MIO2_500	MIO2_UART0_RX_BT_HCI_TX	Wi-Fi / BT	U2	8
U5	PS_MIO3_500	MIO3_UART0_TX_BT_HCI_RX		U2	9
V3	PS_MIO8_500	MIO8_RADIO_EN		U2	19

Table 2 – PS MIO Bank 501 (1.8V, MIOs 26 to 51)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
D10	PS_MIO36_501	MIO36_PS_GPIO1_0	96Boards Low Speed Expansion Connector	J5	23
E11	PS_MIO37_501	MIO37_PS_GPIO1_1		J5	24
C9	PS_MIO38_501	MIO38_SPI0_SCLK		J5	8
C10	PS_MIO39_501	MIO39_PS_GPIO1_2		J5	25
D11	PS_MIO40_501	MIO40_PS_GPIO1_3		J5	26
B10	PS_MIO41_501	MIO41_SPI0_CS		J5	12
D12	PS_MIO42_501	MIO42_SPI0_MISO		J5	10
E13	PS_MIO43_501	MIO43_SPI0_MOSI		J5	14
B11	PS_MIO44_501	MIO44_PS_GPIO1_4		J5	27
A11	PS_MIO45_501	MIO45_PS_GPIO1_5		J5	28
F12	PS_MIO32_501	MIO32	Board ID Strap	JT9	2
E9	PS_MIO33_501	MIO33		JT8	2
E10	PS_MIO35_501	MIO35		JT7	2
G11	PS_MIO27_501	MIO27_DP_AUX_OUT	DisplayPort Signal Transceiver	U10	6
G12	PS_MIO28_501	MIO28_DP_HPD		U10	9
F9	PS_MIO29_501	MIO29_DP_OE		U10	7
G10	PS_MIO30_501	MIO30_DP_AUX_IN		U10	8
F11	PS_MIO31_501	MIO31_MHTN_ALRT	Manhattan PMIC	U21	17
G9	PS_MIO26_501	MIO26_PWR_INT	On/Off Controller	U6	11
F13	PS_MIO34_501	MIO34_POWER_KILL_N		U6	10
C12	PS_MIO46_501	MIO46_SD1_D0	Wi-Fi / BT	U2	24
B12	PS_MIO47_501	MIO47_SD1_D1		U2	25
A12	PS_MIO48_501	MIO48_SD1_D2		U2	26
D13	PS_MIO49_501	MIO49_SD1_D3		U2	27
A13	PS_MIO50_501	MIO50_SD1_CMD		U2	23
C13	PS_MIO51_501	MIO51_SD1_CLK		U2	22

Table 3 – PS MIO Bank 502 (1.8V, MIOs 52 to 77)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
B18	PS_MIO77_502	MIO77_PWR_ALERT_N	Manhattan PMIC	U11	17
G14	PS_MIO52_502	MIO52_USB0_CLK	USB 2.0 PHY to USB 3.0 Device	U14	1
F14	PS_MIO53_502	MIO53_USB0_DIR		U14	31
G15	PS_MIO54_502	MIO54_USB0_DATA2		U14	5
C14	PS_MIO55_502	MIO55_USB0_NXT		U14	2
E14	PS_MIO56_502	MIO56_USB0_DATA0		U14	3
B14	PS_MIO57_502	MIO57_USB0_DATA1		U14	4
A14	PS_MIO58_502	MIO58_USB0_STP		U14	29
E15	PS_MIO59_502	MIO59_USB0_DATA3		U14	6
D15	PS_MIO60_502	MIO60_USB0_DATA4		U14	7
G16	PS_MIO61_502	MIO61_USB0_DATA5		U14	9
C15	PS_MIO62_502	MIO62_USB0_DATA6		U14	10
F16	PS_MIO63_502	MIO63_USB0_DATA7		U14	13
E16	PS_MIO64_502	MIO64_USB1_CLK	USB 2.0 PHY to USB Hub	U4	1
B15	PS_MIO65_502	MIO65_USB1_DIR		U4	31
D16	PS_MIO66_502	MIO66_USB1_DATA2		U4	5
G17	PS_MIO67_502	MIO67_USB1_NXT		U4	2
B16	PS_MIO68_502	MIO68_USB1_DATA0		U4	3
A16	PS_MIO69_502	MIO69_USB1_DATA1		U4	4
A17	PS_MIO70_502	MIO70_USB1_STP		U4	29
F17	PS_MIO71_502	MIO71_USB1_DATA3		U4	6
C17	PS_MIO72_502	MIO72_USB1_DATA4		U4	7
D17	PS_MIO73_502	MIO73_USB1_DATA5		U4	9
D18	PS_MIO74_502	MIO74_USB1_DATA6		U4	10
B17	PS_MIO75_502	MIO75_USB1_DATA7		U4	13
F18	PS_MIO76_502	MIO76_WLAN_IRQ	Wi-Fi / BT	U2	33

5.1.3 Other PS IOs (Banks 503, 504, 505)

Additionally, the ZU+ PS provides three additional I/O banks for the DDR, Config, and transceiver I/Os.

- One Config I/O bank (Bank 503)
  - 11 I/Os connected
  - VCCO = +VCC_PSAUX = 1.8V
  -
- One DDR I/O bank (Bank 504)
  - 64 I/Os connected
  - VCCO = +VCCO_PSDDR = 1.1V

- One Transceiver I/O bank (Bank 505)
  - 16 I/Os connected
  - +MGTRAVCC = 0.85V
  - +MGTRAVTT = 1.8V

Table 4 – PS MIO Bank 503 (1.8V)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
K12	PS_POR_B_503	POWER_GOOD	96Boards Low Speed Expansion Connector	J5	6
J16	PS_MODE0_503	PS_MODE0	Boot Mode DIP Switch	SW3	1
H15	PS_MODE1_503	PS_MODE1	Boot Mode DIP Switch and USB Reset Logic	U15	2
J15	PS_MODE2_503	PS_MODE2	Boot Mode DIP Switch	SW3	2
H18	PS_MODE3_503	PS_MODE3	Boot Mode DIP Switch	R15	1
K13	PS_SRST_B_503	PS_SRST_N	JTAG Header	J3	6
H17	PS_PADI_503	PS_PAD_IN	MPSoC RTC Crystal	X1	2
J17	PS_PADO_503	PS_PAD_OUT		X1	1
K15	PS_INIT_B_503	PS_INIT_N	PS INIT and DONE LEDs	Q4	4
H14	PS_REF_CLK_503	PS_REF_CLK	System Reference Clock	U5	14
K16	PS_ERROR_OUT_503	PS_ERR_OUT	Testpoint	TP4	
K18	PS_ERROR_STATUS_503	PS_ERR_STAT		TP5	

Table 5 – PS DDR IO Bank 504 (1.1V)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
T19	PS_DDR_ZQ_504	NetR23_2	LPDDR4	R23	2
AA22	PS_DDR_A00_504	PS_DDR_CAA0		U13	H2
AB20	PS_DDR_A01_504	PS_DDR_CAA1		U13	J2
AB17	PS_DDR_A02_504	PS_DDR_CAA2		U13	H9
AB19	PS_DDR_A03_504	PS_DDR_CAA3		U13	H10
AB21	PS_DDR_A04_504	PS_DDR_CAA4		U13	H11
AB16	PS_DDR_A05_504	PS_DDR_CAA5		U13	J11
Y21	PS_DDR_A10_504	PS_DDR_CAB0		U13	R2
AA21	PS_DDR_A11_504	PS_DDR_CAB1		U13	P2
AA18	PS_DDR_A12_504	PS_DDR_CAB2		U13	R9
AA19	PS_DDR_A13_504	PS_DDR_CAB3		U13	R10
AA17	PS_DDR_A14_504	PS_DDR_CAB4		U13	R11
AA16	PS_DDR_A15_504	PS_DDR_CAB5		U13	P11
W20	PS_DDR_CK_N0_504	PS_DDR_CKA_C		U13	J9
V20	PS_DDR_CK0_504	PS_DDR_CKA_T		U13	J8
V19	PS_DDR_CK_N1_504	PS_DDR_CKB_C		U13	P9
V18	PS_DDR_CK1_504	PS_DDR_CKB_T		U13	P8
U22	PS_DDR_CKE0_504	PS_DDR_CKE0		U13	J4
V22	PS_DDR_CS_N0_504	PS_DDR_CS0_N		U13	H4
U20	PS_DDR_CS_N1_504	PS_DDR_CS1_N		U13	H3
AB9	PS_DDR_DM0_504	PS_DDR_DMA0		U13	C3
AB14	PS_DDR_DM1_504	PS_DDR_DMA1		U13	C10
U9	PS_DDR_DM2_504	PS_DDR_DMB0		U13	Y3
W13	PS_DDR_DM3_504	PS_DDR_DMB1		U13	Y10
AB11	PS_DDR_DQ0_504	PS_DDR_DQ0		U13	B2
Y10	PS_DDR_DQ1_504	PS_DDR_DQ1		U13	C2
AA12	PS_DDR_DQ10_504	PS_DDR_DQ10		U13	E11
AB12	PS_DDR_DQ11_504	PS_DDR_DQ11		U13	F11
Y14	PS_DDR_DQ12_504	PS_DDR_DQ12		U13	F9
AA14	PS_DDR_DQ13_504	PS_DDR_DQ13		U13	E9
Y15	PS_DDR_DQ14_504	PS_DDR_DQ14		U13	C9
AB15	PS_DDR_DQ15_504	PS_DDR_DQ15		U13	B9
W8	PS_DDR_DQ16_504	PS_DDR_DQ16		U13	AA2
W7	PS_DDR_DQ17_504	PS_DDR_DQ17		U13	Y2

V7	PS_DDR_DQ18_504	PS_DDR_DQ18	LPDDR4	U13	V2
V10	PS_DDR_DQ19_504	PS_DDR_DQ19		U13	U2
AB10	PS_DDR_DQ2_504	PS_DDR_DQ2		U13	E2
U7	PS_DDR_DQ20_504	PS_DDR_DQ20		U13	U4
T9	PS_DDR_DQ21_504	PS_DDR_DQ21		U13	V4
U10	PS_DDR_DQ22_504	PS_DDR_DQ22		U13	Y4
T10	PS_DDR_DQ23_504	PS_DDR_DQ23		U13	AA4
U11	PS_DDR_DQ24_504	PS_DDR_DQ24		U13	AA11
U12	PS_DDR_DQ25_504	PS_DDR_DQ25		U13	Y11
W12	PS_DDR_DQ26_504	PS_DDR_DQ26		U13	V11
W11	PS_DDR_DQ27_504	PS_DDR_DQ27		U13	U11
V14	PS_DDR_DQ28_504	PS_DDR_DQ28		U13	U9
U14	PS_DDR_DQ29_504	PS_DDR_DQ29		U13	V9
W10	PS_DDR_DQ3_504	PS_DDR_DQ3		U13	F2
W15	PS_DDR_DQ30_504	PS_DDR_DQ30		U13	Y9
V15	PS_DDR_DQ31_504	PS_DDR_DQ31		U13	AA9
AA8	PS_DDR_DQ4_504	PS_DDR_DQ4		U13	F4
Y8	PS_DDR_DQ5_504	PS_DDR_DQ5		U13	E4
AB7	PS_DDR_DQ6_504	PS_DDR_DQ6		U13	C4
AA7	PS_DDR_DQ7_504	PS_DDR_DQ7		U13	B4
AA11	PS_DDR_DQ8_504	PS_DDR_DQ8		U13	B11
Y11	PS_DDR_DQ9_504	PS_DDR_DQ9		U13	C11
AA9	PS_DDR_DQS_N0_504	PS_DDR_DQSA0_C		U13	E3
Y9	PS_DDR_DQS_P0_504	PS_DDR_DQSA0_T		U13	D3
AA13	PS_DDR_DQS_N1_504	PS_DDR_DQSA1_C		U13	E10
Y13	PS_DDR_DQS_P1_504	PS_DDR_DQSA1_T		U13	D10
V8	PS_DDR_DQS_N2_504	PS_DDR_DQSB0_C		U13	V3
V9	PS_DDR_DQS_P2_504	PS_DDR_DQSB0_T		U13	W3
V13	PS_DDR_DQS_N3_504	PS_DDR_DQSB1_C		U13	V10
V12	PS_DDR_DQS_P3_504	PS_DDR_DQSB1_T		U13	W10
T18	PS_DDR_RAM_RST_N_504	PS_DDR_RST_N		U13	T11
U21	PS_DDR_CKE1_504	PS_DDR_CKE1		U13	P5/J5
N18	PS_DDR_DQ70_504	NetU1_N18	No Connect	none	none
N19	PS_DDR_DQ71_504	NetU1_N19		none	none
P18	PS_DDR_DQ69_504	NetU1_P18		none	none
P20	PS_DDR_DQS_P8_504	NetU1_P20		none	none
P21	PS_DDR_DQ67_504	NetU1_P21		none	none
P22	PS_DDR_DQ65_504	NetU1_P22		none	none
R18	PS_DDR_DQ68_504	NetU1_R18		none	none
R19	PS_DDR_DM8_504	NetU1_R19		none	none

R20	PS_DDR_DQS_N8_504	NetU1_R20	No Connect	none	none
R21	PS_DDR_DQ66_504	NetU1_R21		none	none
T21	PS_DDR_ALERT_N_504	NetU1_T21		none	none
T22	PS_DDR_DQ64_504	NetU1_T22		none	none
U15	PS_DDR_ACT_N_504	NetU1_U15		none	none
U16	PS_DDR_BG0_504	NetU1_U16		none	none
U17	PS_DDR_BA0_504	NetU1_U17		none	none
U19	PS_DDR_PARITY_504	NetU1_U19		none	none
V17	PS_DDR_BA1_504	NetU1_V17		none	none
W16	PS_DDR_A17_504	NetU1_W16		none	none
W17	PS_DDR_A08_504	NetU1_W17		none	none
W18	PS_DDR_BG1_504	NetU1_W18		none	none
W21	PS_DDR_ODT1_504	NetU1_W21		none	none
W22	PS_DDR_ODT0_504	NetU1_W22		none	none
Y16	PS_DDR_A16_504	NetU1_Y16		none	none
Y18	PS_DDR_A09_504	NetU1_Y18		none	none
Y19	PS_DDR_A07_504	NetU1_Y19		none	none
Y20	PS_DDR_A06_504	NetU1_Y20		none	none

Table 6 – PS Transceiver IO Bank 505

(+MGTRAVCC = 0.85V, +MGTRAVTT = 1.8V)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
J20	PS_MGTREFCLK1N_505	U27M_N	DisplayPort Clock Reference	U5	16
J19	PS_MGTREFCLK1P_505	U27M_P		U5	17
K22	PS_MGTRTXN0_505	GTR_LANE0_TX_N	DisplayPort Connector	J6	11
K21	PS_MGTRTXP0_505	GTR_LANE0_TX_P		J6	9
F22	PS_MGTRTXN1_505	GTR_LANE1_TX_N		J6	5
F21	PS_MGTRTXP1_505	GTR_LANE1_TX_P		J6	3
M20	PS_MGTRREF_505	NetR22_2	MGT Ground Reference	R22	2
L20	PS_MGTREFCLK0N_505	U26M_N	USB 3.0 Clock Reference	U5	19
L19	PS_MGTREFCLK0P_505	U26M_P		U5	20
D22	PS_MGTRRXN2_505	GTR_LANE2_RX_N	USB 3.0 Device Micro A/B	J7	9
D21	PS_MGTRRXP2_505	GTR_LANE2_RX_P		J7	10
C20	PS_MGTRTXN2_505	GTR_LANE2_TX_N		J7	6
C19	PS_MGTRTXP2_505	GTR_LANE2_TX_P		J7	7
B22	PS_MGTRRXN3_505	GTR_LANE3_RX_N	USB 3.1 Hub	U16	48
B21	PS_MGTRRXP3_505	GTR_LANE3_RX_P		U16	47
A20	PS_MGTRTXN3_505	GTR_LANE3_TX_N		U16	51
A19	PS_MGTRTXP3_505	GTR_LANE3_TX_P		U16	50
E19	PS_MGTREFCLK3P_505	NetU1_E19	No Connect	none	none
E20	PS_MGTREFCLK3N_505	NetU1_E20		none	none
G19	PS_MGTREFCLK2P_505	NetU1_G19		none	none
G20	PS_MGTREFCLK2N_505	NetU1_G20		none	none
H21	PS_MGTRRXP1_505	NetU1_H21		none	none
H22	PS_MGTRRXN1_505	NetU1_H22		none	none
M21	PS_MGTRRXP0_505	NetU1_M21		none	none
M22	PS_MGTRRXN0_505	NetU1_M22		none	none

5.1.4 Programmable Logic

- System Logic Cells 154,350
- CLB Flip-Flops 141,120
- CLB LUTs 70,560
- Distributed RAM (Mb) 1.8
- Block RAM Blocks 216
- Block RAM (Mb) 7.6
- UltraRAM Blocks 0
- UltraRAM (Mb) 0
- DSP Slices 360
- CMTs 3
- System Monitor 2

The Zynq UltraScale+ MPSoC Programable Logic (PL) provides two types of I/O banks: High-density (HD) banks and high-performance (HP) banks. The ZU3EG device on the Ultra96-V2 provides:

- One HD bank
  - Bank 26
    - 22 I/Os connected
    - VCCO_26 = +VCCAUX = 1.8V

- Two HP banks
  - Bank 65
    - 29 I/Os connected
    - VCCO_65 = +VCCO_HP = 1.2V
  - Bank 66
    - 2 I/Os connected
    - VCCO_66 → Bank 66 is powered off the Bank 65 VCCO rail
      - VCCO_65 = VCCO_66 = +VCCO_HP = 1.2V
      - See Xilinx AR# 67755

The PL I/Os on Ultra96-V2 are tied to the 96Boards Low-Speed Mezzanine, the 96Boards High-Speed Mezzanine, Bluetooth module, and the fan control.

Table 7 – HD PL IO Bank 26 (1.8V)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
E8	IO_L6P_HDGC_AD6P_26	CSI0_MCLK	96Boards High Speed Expansion Connector	J4	15
D8	IO_L6N_HDGC_AD6N_26	CSI1_MCLK		J4	17
D7	IO_L5P_HDGC_AD7P_26	HD_GPIO_0	96Boards Low Speed Expansion Connector	J5	3
F8	IO_L4P_AD8P_26	HD_GPIO_1		J5	5
E5	IO_L3N_AD9N_26	HD_GPIO_10		J5	18
D6	IO_L5N_HDGC_AD7N_26	HD_GPIO_11		J5	20
D5	IO_L7P_HDGC_AD5P_26	HD_GPIO_12		J5	22
C7	IO_L8N_HDGC_AD4N_26	HD_GPIO_13		J5	30
B6	IO_L11P_AD1P_26	HD_GPIO_14		J5	32
C5	IO_L7N_HDGC_AD5N_26	HD_GPIO_15		J5	34
F7	IO_L4N_AD8N_26	HD_GPIO_2		J5	7
G7	IO_L2P_AD10P_26	HD_GPIO_3		J5	9
F6	IO_L2N_AD10N_26	HD_GPIO_4		J5	11
G5	IO_L1N_AD11N_26	HD_GPIO_5		J5	13
A6	IO_L12N_AD0N_26	HD_GPIO_6		J5	29
A7	IO_L10N_AD2N_26	HD_GPIO_7		J5	31
G6	IO_L1P_AD11P_26	HD_GPIO_8		J5	33
E6	IO_L3P_AD9P_26	HD_GPIO_9		J5	16
A8	IO_L10P_AD2P_26	NetU1_A8	No Connect	none	none
C8	IO_L8P_HDGC_AD4P_26	NetU1_C8		none	none
A9	IO_L9N_AD3N_26	RADIO_LED0	Radio LEDs	Q6	2
B9	IO_L9P_AD3P_26	RADIO_LED1		Q6	5
B5	IO_L11N_AD1N_26	BT_HCI_CTS	Wi-Fi / BT	U2	11
B7	IO_L12P_AD0P_26	BT_HCI_RTS		U2	10

Table 8 – HP PL IO Bank 65 (1.2V)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
P1	IO_L7N_T1L_N1_QBC_AD13N_65	CSI0_C_N	96Boards High Speed Expansion Connector	J4	4
N2	IO_L7P_T1L_N0_QBC_AD13P_65	CSI0_C_P		J4	2
N4	IO_L8N_T1L_N3_AD5N_65	CSI0_D0_N		J4	10
N5	IO_L8P_T1L_N2_AD5P_65	CSI0_D0_P		J4	8
M1	IO_L9N_T1L_N5_AD12N_65	CSI0_D1_N		J4	16
M2	IO_L9P_T1L_N4_AD12P_65	CSI0_D1_P		J4	14
M4	IO_L10N_T1U_N7_QBC_AD4N_65	CSI0_D2_N		J4	22
M5	IO_L10P_T1U_N6_QBC_AD4P_65	CSI0_D2_P		J4	20
L1	IO_L11N_T1U_N9_GC_65	CSI0_D3_N		J4	28
L2	IO_L11P_T1U_N8_GC_65	CSI0_D3_P		J4	26
T2	IO_L1N_T0L_N1_DBC_65	CSI1_C_N		J4	56
T3	IO_L1P_T0L_N0_DBC_65	CSI1_C_P		J4	54
R3	IO_L2N_T0L_N3_65	CSI1_D0_N		J4	44
P3	IO_L2P_T0L_N2_65	CSI1_D0_P		J4	42
U1	IO_L3N_T0L_N5_AD15N_65	CSI1_D1_N		J4	50
U2	IO_L3P_T0L_N4_AD15P_65	CSI1_D1_P		J4	48
H5	IO_L16N_T2U_N7_QBC_AD3N_65	DSI_CLK_N		J4	23
J5	IO_L16P_T2U_N6_QBC_AD3P_65	DSI_CLK_P		J4	21
F1	IO_L19N_T3L_N1_DBC_AD9N_65	DSI_D0_N		J4	29
G1	IO_L19P_T3L_N0_DBC_AD9P_65	DSI_D0_P		J4	27
E3	IO_L20N_T3L_N3_AD1N_65	DSI_D1_N		J4	35
E4	IO_L20P_T3L_N2_AD1P_65	DSI_D1_P		J4	33
D1	IO_L21N_T3L_N5_AD8N_65	DSI_D2_N		J4	41
E1	IO_L21P_T3L_N4_AD8P_65	DSI_D2_P		J4	39
C3	IO_L22N_T3U_N7_DBC_AD0N_65	DSI_D3_N		J4	47
D3	IO_L22P_T3U_N6_DBC_AD0P_65	DSI_D3_P		J4	45
C2	IO_L24N_T3U_N11_PERSTN0_65	HSIC_DATA		J4	59
F4	IO_T3U_N12_65	FAN_PWM	Fan PWM	Q9	1
P2	IO_T0U_N12_VRP_65	NetR35_1	VRP	R35	2
D2	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	NetU1_D2	No Connect	none	none
F2	IO_L23N_T3U_N9_65	NetU1_F2		none	none
F3	IO_L23P_T3U_N8_I2C_SCLK_65	NetU1_F3		none	none
G2	IO_L17N_T2U_N9_AD10N_65	NetU1_G2		none	none
G4	IO_L18N_T2U_N11_AD2N_65	NetU1_G4		none	none

H2	IO_L17P_T2U_N8_AD10P_65	NetU1_H2		none	none
H3	IO_T2U_N12_65	NetU1_H3		none	none
H4	IO_L18P_T2U_N10_AD2P_65	NetU1_H4		none	none
J1	IO_L15N_T2L_N5_AD11N_65	NetU1_J1		none	none
J2	IO_L13N_T2L_N1_GC_QBC_65	NetU1_J2		none	none
J3	IO_L13P_T2L_N0_GC_QBC_65	NetU1_J3		none	none
K1	IO_L15P_T2L_N4_AD11P_65	NetU1_K1		none	none
K3	IO_L14N_T2L_N3_GC_65	NetU1_K3		none	none
K4	IO_L14P_T2L_N2_GC_65	NetU1_K4		none	none
K5	VREF_65	NetU1_K5		none	none
L3	IO_L12N_T1U_N11_GC_65	NetU1_L3		none	none
L4	IO_L12P_T1U_N10_GC_65	NetU1_L4		none	none
N3	IO_T1U_N12_65	NetU1_N3		none	none
P5	IO_L6P_T0U_N10_AD6P_65	NetU1_P5		none	none
R1	IO_L5P_T0U_N8_AD14P_65	NetU1_R1		none	none
R4	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	NetU1_R4		none	none
R5	IO_L6N_T0U_N11_AD6N_65	NetU1_R5		none	none
T1	IO_L5N_T0U_N9_AD14N_65	NetU1_T1		none	none
T4	IO_L4N_T0U_N7_DBC_AD7N_65	NetU1_T4		none	none

Table 9 – HP PL IO Bank 66 (1.2V)

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
				REFDES	REFDES Pin Number
A2	IO_T3U_N12_66	HSIC_STR	96Boards High Speed Expansion Connector	J4	57
A3	IO_L12N_T1U_N11_GC_66	NetJT5_3	Radio Reset: MIO or PL Select	JT5	3
A4	IO_L12P_T1U_N10_GC_66	NetU1_A4	No Connect	none	none
B1	IO_L11N_T1U_N9_GC_66	NetU1_B1	No Connect	none	none
B2	IO_L11P_T1U_N8_GC_66	NetU1_B2	No Connect	none	none
B4	IO_T0U_N12_VRP_66	NetU1_B4	No Connect	none	none
C4	VREF_66	NetU1_C4	No Connect	none	none

5.2 LPDDR4 Memory

Ultra96-V2 provides 2GB (512Mbit x 32) of 533MHz (1066Mbps) LPDDR4 memory using a single-die Micron MT53D512M32D2DS-053 AIT:D.

The memory device is a 0.53 ns (1866 MHz) speed grade. However, that is irrelevant as the interface clocking is set by the MPSoC package as 533 MHz maximum. This can be found in Xilinx document DS925 (as seen in Table 30 of DS925 v1.17 March 13, 2020).

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade				Units
			-3E -2E/-2LE -1E		-2I/-2LI -1I/-1M/-1Q -1LI		
			Min	Max	Min	Max	
DDR4[4]	All FFV and FFR packages, FBVB900, SFVC784, and SFRC784	Single rank component	664	2400	1000	2400	Mb/s
		2 rank DIMM[1, 3]	664	1066	1000	1066	Mb/s
LPDDR4[5]	All FFV and FFR packages, FBVB900, SFVC784, and SFRC784	Single die package[6, 7]	664	2400	1000	2400	Mb/s
		Dual die package[6, 7]	664	2133	1000	2133	Mb/s
	SFVA625	Single die package[6, 7]	664	2133	1000	2133	Mb/s
		Dual die package[6, 7]	664	1866	1000	1866	Mb/s
	SBVA484	Single die package[6, 7]	664	1066	1000	1066	Mb/s
		Dual die package[6, 7]	664	1066	1000	1066	Mb/s

Additionally, the temperature grade for the LPDDR4 on the V2 is industrial, meaning the same device is populated on both the C- and I-grade Ultra96-V2 SBC.

5.2.1 Comparison with Ultra96-V1 LPDDR4

The Ultra96-V1 had a dual-die device which is now EOL. The Ultra96-V2's single-die device has the exact same capacity and timing parameters. However, the difference in die quantity shows up as a Rank and Addressing change in the ZU+ PS DDR controller parameters, which affects the designs at the FSBL level.

The other key differences are the speed grade and temperature grade. The V2's LPDDR4 speed-grade is faster, but that is irrelevant since the LPDDR4 interface is limited by the Xilinx Zynq UltraScale+ MPSoC package. The faster speed-grade was selected based on availability. Additionally, the temperature grade for the LPDDR4 on the V2 is I-grade, making it possible for us to support the I-grade temp Ultra96-V2.

These are the MPSoC PS DDR controller differences on the Ultra96-V2's Micron LPDDR4 (MT53D512M32D2DS-053 AIT:D) compared to Ultra96-V1's LPDDR4 (MT53B512M32D2NP-062 WT:C).

```
<user_parameter name="CONFIG.PSU__DDRC__DEVICE_CAPACITY" value="16384 MBits"/>

<user_parameter name="CONFIG.PSU__DDRC__RANK_ADDR_COUNT" value="0"/>

<user_parameter name="CONFIG.PSU__DDRC__ROW_ADDR_COUNT"  value="16"/>
```

This is how those parameters look in Vivado block design:

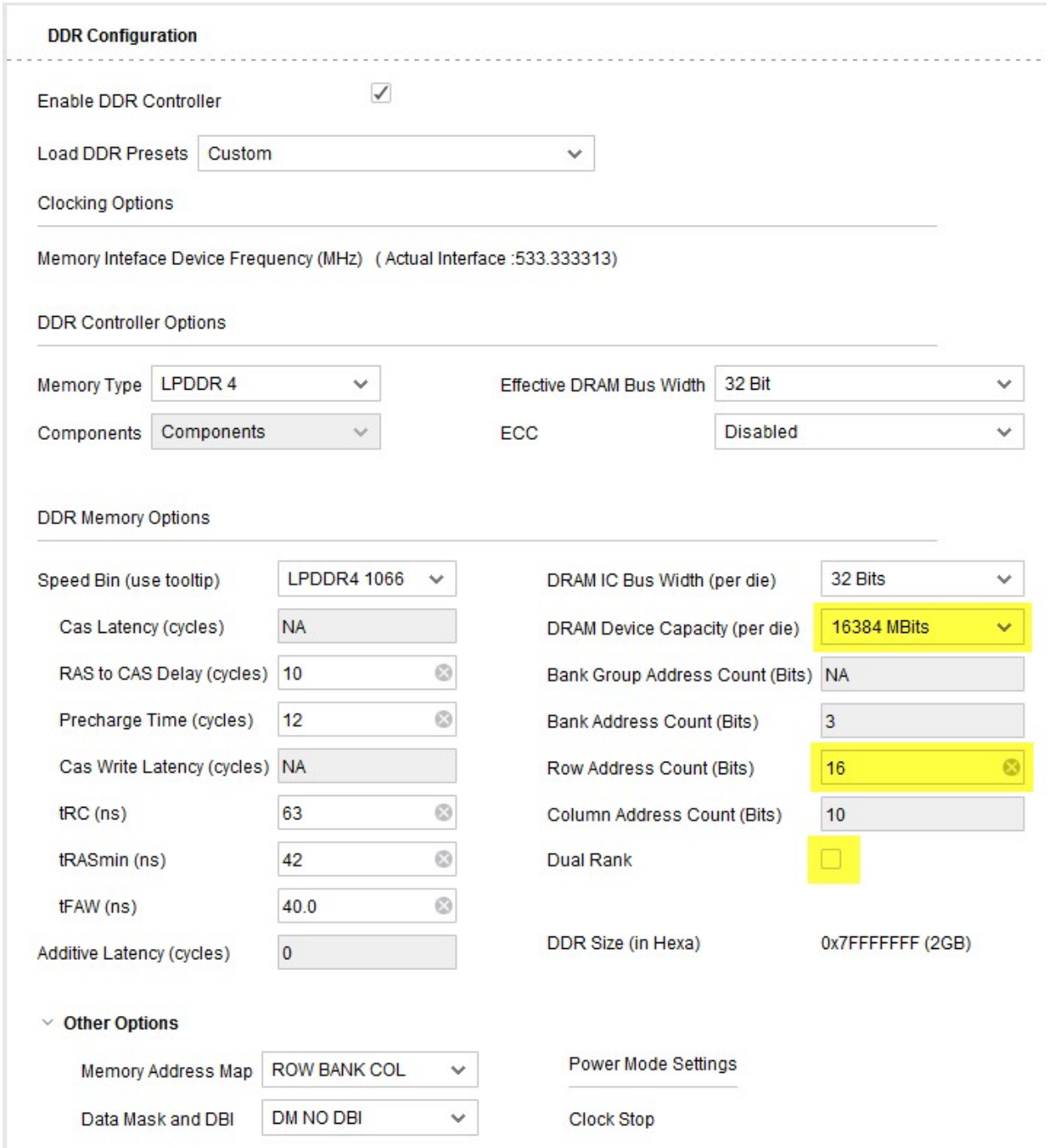


Figure 4 – Ultra96-V2 PS DDR Controller Settings (Differences with Ultra96-V1 Highlighted)

5.2.2 LPDDR4 Pin Table

The table below shows the pin connections for the LPDDR4 on Ultra96-V2

Table 10 – LPDDR4 Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	Connects to:	
				REFDES	REFDES Pin Number
T19	504	PS_DDR_ZQ_504	NetR23_2	R23	2
AA22	504	PS_DDR_A00_504	PS_DDR_CAA0	U13	H2
AB20	504	PS_DDR_A01_504	PS_DDR_CAA1	U13	J2
AB17	504	PS_DDR_A02_504	PS_DDR_CAA2	U13	H9
AB19	504	PS_DDR_A03_504	PS_DDR_CAA3	U13	H10
AB21	504	PS_DDR_A04_504	PS_DDR_CAA4	U13	H11
AB16	504	PS_DDR_A05_504	PS_DDR_CAA5	U13	J11
Y21	504	PS_DDR_A10_504	PS_DDR_CAB0	U13	R2
AA21	504	PS_DDR_A11_504	PS_DDR_CAB1	U13	P2
AA18	504	PS_DDR_A12_504	PS_DDR_CAB2	U13	R9
AA19	504	PS_DDR_A13_504	PS_DDR_CAB3	U13	R10
AA17	504	PS_DDR_A14_504	PS_DDR_CAB4	U13	R11
AA16	504	PS_DDR_A15_504	PS_DDR_CAB5	U13	P11
W20	504	PS_DDR_CK_N0_504	PS_DDR_CKA_C	U13	J9
V20	504	PS_DDR_CK0_504	PS_DDR_CKA_T	U13	J8
V19	504	PS_DDR_CK_N1_504	PS_DDR_CKB_C	U13	P9
V18	504	PS_DDR_CK1_504	PS_DDR_CKB_T	U13	P8
U22	504	PS_DDR_CKE0_504	PS_DDR_CKE0	U13	J4
V22	504	PS_DDR_CS_N0_504	PS_DDR_CS0_N	U13	H4
U20	504	PS_DDR_CS_N1_504	PS_DDR_CS1_N	U13	H3
AB9	504	PS_DDR_DM0_504	PS_DDR_DMA0	U13	C3
AB14	504	PS_DDR_DM1_504	PS_DDR_DMA1	U13	C10
U9	504	PS_DDR_DM2_504	PS_DDR_DMB0	U13	Y3
W13	504	PS_DDR_DM3_504	PS_DDR_DMB1	U13	Y10
AB11	504	PS_DDR_DQ0_504	PS_DDR_DQ0	U13	B2
Y10	504	PS_DDR_DQ1_504	PS_DDR_DQ1	U13	C2
AB10	504	PS_DDR_DQ2_504	PS_DDR_DQ2	U13	E2
W10	504	PS_DDR_DQ3_504	PS_DDR_DQ3	U13	F2
AA8	504	PS_DDR_DQ4_504	PS_DDR_DQ4	U13	F4
Y8	504	PS_DDR_DQ5_504	PS_DDR_DQ5	U13	E4
AB7	504	PS_DDR_DQ6_504	PS_DDR_DQ6	U13	C4

AA7	504	PS_DDR_DQ7_504	PS_DDR_DQ7	U13	B4
AA11	504	PS_DDR_DQ8_504	PS_DDR_DQ8	U13	B11
Y11	504	PS_DDR_DQ9_504	PS_DDR_DQ9	U13	C11
AA12	504	PS_DDR_DQ10_504	PS_DDR_DQ10	U13	E11
AB12	504	PS_DDR_DQ11_504	PS_DDR_DQ11	U13	F11
Y14	504	PS_DDR_DQ12_504	PS_DDR_DQ12	U13	F9
AA14	504	PS_DDR_DQ13_504	PS_DDR_DQ13	U13	E9
Y15	504	PS_DDR_DQ14_504	PS_DDR_DQ14	U13	C9
AB15	504	PS_DDR_DQ15_504	PS_DDR_DQ15	U13	B9
W8	504	PS_DDR_DQ16_504	PS_DDR_DQ16	U13	AA2
W7	504	PS_DDR_DQ17_504	PS_DDR_DQ17	U13	Y2
V7	504	PS_DDR_DQ18_504	PS_DDR_DQ18	U13	V2
V10	504	PS_DDR_DQ19_504	PS_DDR_DQ19	U13	U2
U7	504	PS_DDR_DQ20_504	PS_DDR_DQ20	U13	U4
T9	504	PS_DDR_DQ21_504	PS_DDR_DQ21	U13	V4
U10	504	PS_DDR_DQ22_504	PS_DDR_DQ22	U13	Y4
T10	504	PS_DDR_DQ23_504	PS_DDR_DQ23	U13	AA4
U11	504	PS_DDR_DQ24_504	PS_DDR_DQ24	U13	AA11
U12	504	PS_DDR_DQ25_504	PS_DDR_DQ25	U13	Y11
W12	504	PS_DDR_DQ26_504	PS_DDR_DQ26	U13	V11
W11	504	PS_DDR_DQ27_504	PS_DDR_DQ27	U13	U11
V14	504	PS_DDR_DQ28_504	PS_DDR_DQ28	U13	U9
U14	504	PS_DDR_DQ29_504	PS_DDR_DQ29	U13	V9
W15	504	PS_DDR_DQ30_504	PS_DDR_DQ30	U13	Y9
V15	504	PS_DDR_DQ31_504	PS_DDR_DQ31	U13	AA9
AA9	504	PS_DDR_DQS_N0_504	PS_DDR_DQSA0_C	U13	E3
Y9	504	PS_DDR_DQS_P0_504	PS_DDR_DQSA0_T	U13	D3
AA13	504	PS_DDR_DQS_N1_504	PS_DDR_DQSA1_C	U13	E10
Y13	504	PS_DDR_DQS_P1_504	PS_DDR_DQSA1_T	U13	D10
V8	504	PS_DDR_DQS_N2_504	PS_DDR_DQSB0_C	U13	V3
V9	504	PS_DDR_DQS_P2_504	PS_DDR_DQSB0_T	U13	W3
V13	504	PS_DDR_DQS_N3_504	PS_DDR_DQSB1_C	U13	V10
V12	504	PS_DDR_DQS_P3_504	PS_DDR_DQSB1_T	U13	W10
T18	504	PS_DDR_RAM_RST_N_504	PS_DDR_RST_N	U13	T11

5.3 microSD Card

Ultra96-V2 provides a microSD card socket as the primary boot device. VCCO for the SDIO lines going into the Zynq MPSoC is 1.80V, thus a level shifter (U3, TXS02612RTWR) is required to go from the 3.3V native SD card slot to 1.80V

The microSD card socket J2 is a TE Connectivity 2201778-1. This is a push-push style socket. This socket is one of the two exceptions to the -40C rating on the Ultra96-V2 I-grade since this socket is rated -30C to +85C. This socket has a spring-type mechanism inside that can become brittle at very cold temperatures. If the mechanism is exercised at extremely cold temperatures, the mechanism could break. Avnet did test the Ultra96-V2 I-grade to the full -40C temperature; however, we did not insert/remove the microSD card at -40C. The card was inserted at room temperature, after which the entire Device Under Test was placed in a thermal chamber and then soaked to -40C. Under these conditions, the board passed all testing, and the hardware was not damaged.

If you need an Ultra96-V2 where the power jack or microSD card must be removed or inserted at -40C, Avnet has researched options that will work, but it requires small modifications to the PCB. If this is something you are interested in pursuing, please discuss with your local Avnet FAE or contact customize@avnet.com.

The Ultra96-V2 Single Board Computer ships with a blank Delkin Devices 16 GB Industrial MLC microSD card.

- C-grade Ultra96-V2 SBC
  - Delkin Utility class device
  - Part number S416APG49-U3000-3
- I-grade Ultra96-V2 SBC
  - Delkin Utility+ class device
  - Part number S316APG49-U3000-3
- A micro-SD to SD Adapter is included in both kits

The Delkin Utility/Utility+ cards are rated at Read Performance = 95MB/s and Write Performance = 55MB/s (measured using CrystalDiskMark).

5.3.1 MLC Advantage

There are several advantages to using MLC over the typical retail TLC that is readily available. These advantages are significant, and this explains why an MLC card was specifically chosen for these kits. For more information, refer to this article on the Element14 community: https://www.element14.com/community/groups/embedded/blog/2018/03/26/why-not-all-sd-cards-are-created-equal-storage-insights-1

Table 11 – Comparison of TLC vs. MLC microSD Cards

	Retail TLC	Delkin Utility MLC
CrystalDiskMark Read Performance	80MB/s	95 MB/s
CrystalDiskMark Write Performance	20MB/s	55 MB/s
Lifecycle	<12 months	18-24 months
Endurance (Program/Erase cycles)	300-600	3000
SMART data enabled (card life stats)	No	Yes
Embedded mode – aligned to efficiently work with Linux based OS as opposed to FAT only	No	Yes

5.3.2 microSD Pin Table

The table below shows the pin connections for the microSD circuit on Ultra96-V2.

Table 12 – microSD Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	Connects to:	
				REFDES	REFDES Pin Number
AB6	500	PS_MIO24_500	MIO24_SD0_DETECT	J2	9
W3	500	PS_MIO13_500	MIO13_SD0_DAT0	U3	6
W5	500	PS_MIO14_500	MIO14_SD0_DAT1	U3	7
Y4	500	PS_MIO15_500	MIO15_SD0_DAT2	U3	1
Y3	500	PS_MIO16_500	MIO16_SD0_DAT3	U3	3
W6	500	PS_MIO21_500	MIO21_SD0_CMD	U3	4
AA6	500	PS_MIO22_500	MIO22_SD0_CLK	U3	9

5.4 USB

Ultra96-V2 provides one upstream (device) and two downstream (host) USB 3.0 connections. A USB 2.0 downstream (host) interface is also provided on the HS expansion connector.

Two Microchip USB3320 USB 2.0 ULPI Transceivers and one Microchip USB5744 4-Port SS/HS USB Controller Hub are specified.

Figure 5 below shows the Ultra96-V2 USB circuit connections.

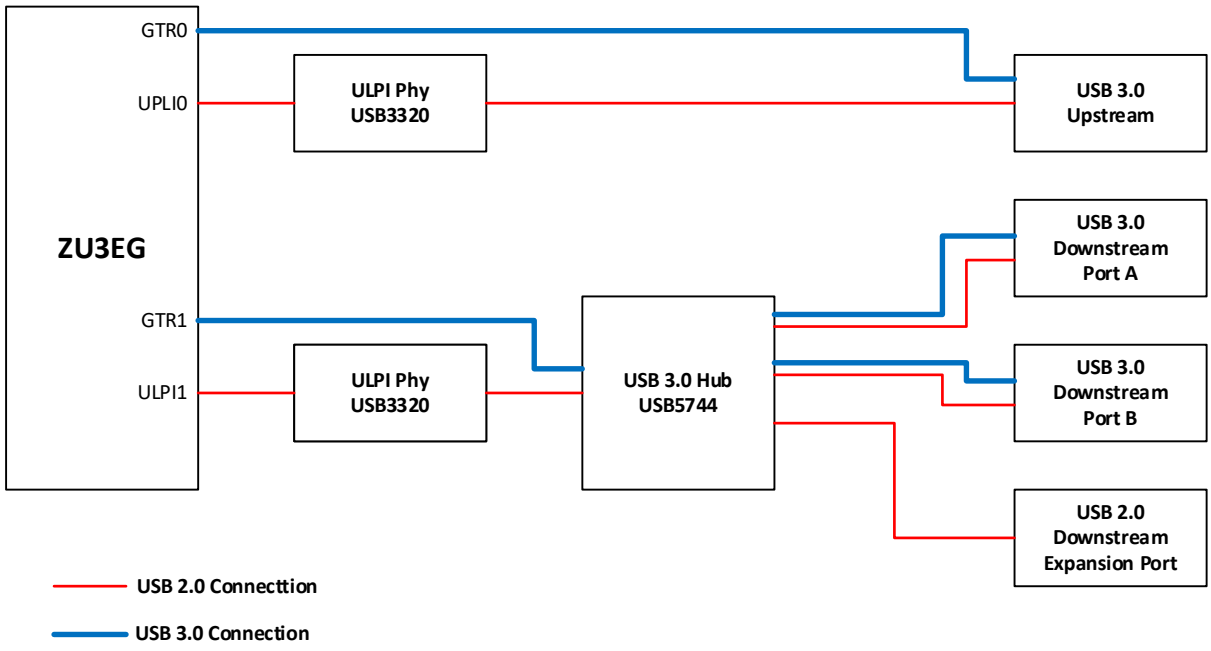


Figure 5 – USB Setup

5.4.1 USB5744 Implementation Details

Refer to the USB5744 datasheet (http://ww1.microchip.com/downloads/en/DeviceDoc/00001855C.pdf) and the EVB-USB5744 Evaluation Board schematics (http://ww1.microchip.com/downloads/en/DeviceDoc/EVB-USB5744_A1-sch.pdf) for implementation details.

NOTE: USB 3.0 Downstream Port A/B VUBS is controlled by a Microchip/Micrel MIC2009YML USB Power Switch following the Evaluation Board implementation

NOTE: USB2.0 Downstream Port VBUS is provided by the Low Speed Expansion Header 5V supply (see 5.12.1). A Power switch is not required and the corresponding USB5744 PRT_CTLx pin for that port is left n/c.

5.4.2 USB Pin Tables

Table 13 – USB 3.0 Clock Reference (26 MHz)

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
					REFDES	REFDES Pin Number
L20	505	PS_MGTREFCLK0N_505	U26M_N	USB 3.0 Clock Reference	U5	19
L19	505	PS_MGTREFCLK0P_505	U26M_P	USB 3.0 Clock Reference	U5	20

Table 14 – USB 3.0 Device

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
					REFDES	REFDES Pin Number
G14	502	PS_MIO52_502	MIO52_USB0_CLK	USB 2.0 PHY to USB 3.0 Device	U14	1
F14	502	PS_MIO53_502	MIO53_USB0_DIR	USB 2.0 PHY to USB 3.0 Device	U14	31
G15	502	PS_MIO54_502	MIO54_USB0_DATA2	USB 2.0 PHY to USB 3.0 Device	U14	5
C14	502	PS_MIO55_502	MIO55_USB0_NXT	USB 2.0 PHY to USB 3.0 Device	U14	2
E14	502	PS_MIO56_502	MIO56_USB0_DATA0	USB 2.0 PHY to USB 3.0 Device	U14	3
B14	502	PS_MIO57_502	MIO57_USB0_DATA1	USB 2.0 PHY to USB 3.0 Device	U14	4
A14	502	PS_MIO58_502	MIO58_USB0_STP	USB 2.0 PHY to USB 3.0 Device	U14	29
E15	502	PS_MIO59_502	MIO59_USB0_DATA3	USB 2.0 PHY to USB 3.0 Device	U14	6
D15	502	PS_MIO60_502	MIO60_USB0_DATA4	USB 2.0 PHY to USB 3.0 Device	U14	7
G16	502	PS_MIO61_502	MIO61_USB0_DATA5	USB 2.0 PHY to USB 3.0 Device	U14	9
C15	502	PS_MIO62_502	MIO62_USB0_DATA6	USB 2.0 PHY to USB 3.0 Device	U14	10
F16	502	PS_MIO63_502	MIO63_USB0_DATA7	USB 2.0 PHY to USB 3.0 Device	U14	13
D22	505	PS_MGTRRXN2_505	GTR_LANE2_RX_N	USB 3.0 Device Micro A/B	J7	9
D21	505	PS_MGTRRXP2_505	GTR_LANE2_RX_P	USB 3.0 Device Micro A/B	J7	10
C20	505	PS_MGTRTXN2_505	GTR_LANE2_TX_N	USB 3.0 Device Micro A/B	J7	6
C19	505	PS_MGTRTXP2_505	GTR_LANE2_TX_P	USB 3.0 Device Micro A/B	J7	7

Table 15 – USB 3.1 Hub

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	Function	Connects to:	
					REFDES	REFDES Pin Number
E16	502	PS_MIO64_502	MIO64_USB1_CLK	USB 2.0 PHY to USB Hub	U4	1
B15	502	PS_MIO65_502	MIO65_USB1_DIR	USB 2.0 PHY to USB Hub	U4	31
D16	502	PS_MIO66_502	MIO66_USB1_DATA2	USB 2.0 PHY to USB Hub	U4	5
G17	502	PS_MIO67_502	MIO67_USB1_NXT	USB 2.0 PHY to USB Hub	U4	2
B16	502	PS_MIO68_502	MIO68_USB1_DATA0	USB 2.0 PHY to USB Hub	U4	3
A16	502	PS_MIO69_502	MIO69_USB1_DATA1	USB 2.0 PHY to USB Hub	U4	4
A17	502	PS_MIO70_502	MIO70_USB1_STP	USB 2.0 PHY to USB Hub	U4	29
F17	502	PS_MIO71_502	MIO71_USB1_DATA3	USB 2.0 PHY to USB Hub	U4	6
C17	502	PS_MIO72_502	MIO72_USB1_DATA4	USB 2.0 PHY to USB Hub	U4	7
D17	502	PS_MIO73_502	MIO73_USB1_DATA5	USB 2.0 PHY to USB Hub	U4	9
D18	502	PS_MIO74_502	MIO74_USB1_DATA6	USB 2.0 PHY to USB Hub	U4	10
B17	502	PS_MIO75_502	MIO75_USB1_DATA7	USB 2.0 PHY to USB Hub	U4	13
B22	505	PS_MGTRRXN3_505	GTR_LANE3_RX_N	USB 3.1 Hub	U16	48
B21	505	PS_MGTRRXP3_505	GTR_LANE3_RX_P	USB 3.1 Hub	U16	47
A20	505	PS_MGTRTXN3_505	GTR_LANE3_TX_N	USB 3.1 Hub	U16	51
A19	505	PS_MGTRTXP3_505	GTR_LANE3_TX_P	USB 3.1 Hub	U16	50

5.5 Wi-Fi / Bluetooth

Ultra96-V2 supports Wi-Fi (802.11b/g/n) and Bluetooth 4.0. A Microchip ATWILC300-MR110CA Single Band Combo Wi-Fi, Bluetooth & Bluetooth low energy module is utilized for these interfaces.

5.5.1 Wi-Fi

The ATWILC300-MR110CA WLAN interface connects to the MPSoC through the Secure Digital SD1 interface. The WLAN interrupt WLAN_IRQ is connected to PS MIO76, the WLAN enable signal RADIO_EN is connected to PS MIO7. A yellow LED is connected to Bank 26 programmable logic and can be used to indicate that Wi-Fi is enabled when configured properly.

5.5.2 Bluetooth

The ATWILC300-MR110CA Bluetooth interface connects through a UART interface. Since the Bluetooth UART interface requires hardware flow-control (RTS/CTS), which is only available through the PL, the UART RX/TX signals are connected to PS UART0 (MIO2, MIO3) and the RTS/CTS signals are connected to the PL High-Density (HD) bank. A blue LED is connected to Bank 26 programmable logic and can be used to indicate that Bluetooth is enabled when configured properly.

5.5.3 Bluetooth Audio

ATWILC300-MR110CA Bluetooth Audio connects through a PCM/I2S interface. Since MPSoC does not provide a PCM/I2S interface, this functionality is provided at test points TP11 – TP19.

5.5.4 Wi-Fi / Bluetooth Pin Table

Table 16 – Wi-Fi / Bluetooth Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	MPSoC VCCO	Connects to:	
					REFDES	REFDES Pin Number
B5	26	IO_L11N_AD1N_26	BT_HCI_CTS	+VCCAUX = 1.8V	U2	11
B7	26	IO_L12P_AD0P_26	BT_HCI_RTS	+VCCAUX = 1.8V	U2	10
V2	500	PS_MIO2_500	MIO2_UART0_RX_BT_HCI_TX	+VCC_PSAUX = 1.8V	U2	8
U5	500	PS_MIO3_500	MIO3_UART0_TX_BT_HCI_RX	+VCC_PSAUX = 1.8V	U2	9
V3	500	PS_MIO8_500	MIO8_RADIO_EN	+VCC_PSAUX = 1.8V	U2	19
C12	501	PS_MIO46_501	MIO46_SD1_D0	+VCC_PSAUX = 1.8V	U2	24
B12	501	PS_MIO47_501	MIO47_SD1_D1	+VCC_PSAUX = 1.8V	U2	25
A12	501	PS_MIO48_501	MIO48_SD1_D2	+VCC_PSAUX = 1.8V	U2	26
D13	501	PS_MIO49_501	MIO49_SD1_D3	+VCC_PSAUX = 1.8V	U2	27
A13	501	PS_MIO50_501	MIO50_SD1_CMD	+VCC_PSAUX = 1.8V	U2	23
C13	501	PS_MIO51_501	MIO51_SD1_CLK	+VCC_PSAUX = 1.8V	U2	22
F18	502	PS_MIO76_502	MIO76_WLAN_IRQ	+VCC_PSAUX = 1.8V	U2	33

5.6 Mini DisplayPort

Ultra96-V2 supports one Mini DisplayPort output. A TE Connectivity 2129320-3 provides the Mini DisplayPort connectivity.

Table 17 -- Mini DisplayPort Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	MPSoC VCCO	Function	Connects to:	
						REFDES	REFDES Pin Number
G11	501	PS_MIO27_501	MIO27_DP_AUX_OUT	+VCC_PSAUX = 1.8V	DisplayPort Signal Transceiver	U10	6
G12	501	PS_MIO28_501	MIO28_DP_HPD	+VCC_PSAUX = 1.8V	DisplayPort Signal Transceiver	U10	9
F9	501	PS_MIO29_501	MIO29_DP_OE	+VCC_PSAUX = 1.8V	DisplayPort Signal Transceiver	U10	7
G10	501	PS_MIO30_501	MIO30_DP_AUX_IN	+VCC_PSAUX = 1.8V	DisplayPort Signal Transceiver	U10	8
J20	505	PS_MGTREFCLK1N_505	U27M_N	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Clock Reference	U5	16
J19	505	PS_MGTREFCLK1P_505	U27M_P	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Clock Reference	U5	17
K22	505	PS_MGTRTXN0_505	GTR_LANE0_TX_N	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Connector	J6	11
K21	505	PS_MGTRTXP0_505	GTR_LANE0_TX_P	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Connector	J6	9
F22	505	PS_MGTRTXN1_505	GTR_LANE1_TX_N	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Connector	J6	5
F21	505	PS_MGTRTXP1_505	GTR_LANE1_TX_P	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Connector	J6	3

5.7 UART

Ultra96-V2 provides access to one UART on the baseboard. PS UART1 (MIO0, MIO1 on Bank 500) is connected to a 4-pin 2mm header (J1). The IO Voltage on the MPSoC is 1.8V, and the signals are routed through a level translator (Q1, Q2) to allow for compatibility with 3.3V.

The J1 UART Header is compatible with the Avnet Ultra96 USB-to-JTAG/UART Pod (AES-ACC-U96-JTAG), which you can purchase as an accessory.

http://avnet.me/ultra96jtag

This pod has an option to either use a default 3.3V I/O voltage or use J1-Pin4 as a reference voltage. The Ultra96-V2 was used to test the JTAG/UART Pod Vref option. To enable that testing, a resistor jumper JT1 was added to enable this testing. However, it is not intended that a normal user will make use of this capability as it requires moving the JT1 resistor to the 2-3 position and also replacing the Q1 and Q2 circuitry with wire shorts.

Since Ultra96-V2 has native level translators (Q1 and Q2) on board, translating from 1.8V to 3.3V, the Ultra96-V2 J1 UART connection is compatible with both the 3-pin and 4-pin JTAG/UART Pods. For more information, read the blog at

http://avnet.me/JTAG-UART-pod-vref

Table 18 – Pinout for UART and J1 Connector

MPSoC Pin Number	MPSoC Site Name	Ultra96-V2 Net name	MPSoC VCCO	Connects to:		Connects to:	
				REFDES	REFDES Pin Number	REFDES	REFDES Pin Number
U4	PS_MIO0_500	MIO0_UART1_TX	+VCC_PSAUX = 1.8V	Q2	2	J1	2
W1	PS_MIO1_500	MIO1_UART1_RX	+VCC_PSAUX = 1.8V	Q1	2	J1	1
N/A	N/A	GND	N/A	N/A	N/A	J1	3
N/A	N/A	UART_VREF	+3.3V or +VCC_PSAUX	JT	2	J1	4

5.8 I2C

Ultra96-V2 supports one I2C bus. A TI TCA9544A Low-Voltage 8-Channel I2C Port Expander is specified to isolate the I2C sub-buses from each other. All I2C buses operate at 1.8V.

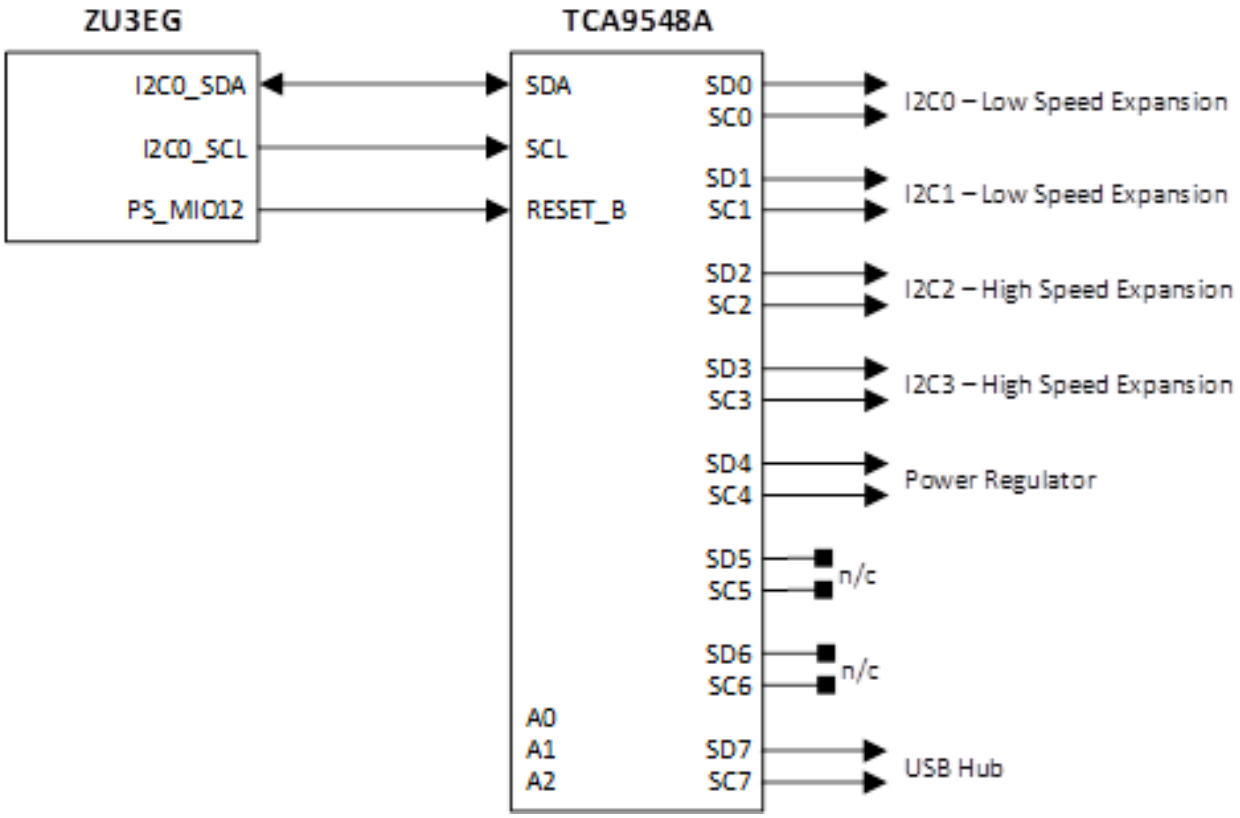


Figure 6 – MPSoC I2C to I2C Port Expander

Table 19 – I2C Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	Connects to:	
				REFDES	REFDES Pin Number
AB2	500	PS_MIO12_500	MIO12_I2C_MUX_RESET_N	U7	24
U6	500	PS_MIO4_500	MIO4_I2C1_SCL	U7	19
AA1	500	PS_MIO5_500	MIO5_I2C1_SDA	U7	20

5.9 LEDs

Ultra96-V2 utilizes 10 OSRAM Opto Semiconductor LEDs for the following functions:

- Green LG Q396-PS-35
  - +3.3V Power Good
  - VIN Power Good
  - Four user-controllable LEDs connected to PS_MIO[17..20].
- Blue LB Q39G-L2OO-35-1
  - User-controllable Radio status connected to PL Pin B9
  - MPSoC DONE
- Red LS Q976-NR-1
  - MPSoC INIT
- Yellow LY Q971-H1K1-36
  - User-controllable Radio status connected to PL Pin A9

Table 20 – LED Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	MPSoC VCCO	Function	Connects to:		Connects to:	
						REFDES	REFDES Pin Number	LED REFDES	Color
A9	26	IO_L9N_AD3N_26	RADIO_LED0	+VCCAUX = 1.8V	Radio LEDs	Q6	2	D9	Yellow
B9	26	IO_L9P_AD3P_26	RADIO_LED1	+VCCAUX = 1.8V	Radio LEDs	Q6	5	D10	Blue
AB4	500	PS_MIO20_500	MIO20_PS_LED0	+VCC_PSAUX = 1.8V	PS LEDs	Q3	2	D3	Green
AA4	500	PS_MIO19_500	MIO19_PS_LED1	+VCC_PSAUX = 1.8V	PS LEDs	Q3	5	D4	Green
Y5	500	PS_MIO18_500	MIO18_PS_LED2	+VCC_PSAUX = 1.8V	PS LEDs	Q5	2	D6	Green
AA3	500	PS_MIO17_500	MIO17_PS_LED3	+VCC_PSAUX = 1.8V	PS LEDs	Q5	5	D7	Green
K15	503	PS_INIT_B_503	PS_INIT_N	+VCC_PSAUX = 1.8V	PS INIT	Q4	4	D5	Red
L12	503	PS_DONE_503	PS_DONE	+VCC_PSAUX = 1.8V	PS DONE	Q4	2	D1	Blue
N/A	N/A	N/A	N/A	N/A	+3.3V LED	R45	2	D2	Green
N/A	N/A	N/A	N/A	N/A	VIN LED	R193	2	D17	Green

5.10 Clocking

Ultra96-V2 provides the following system clocks to the MPSoC:

- PS_CLK: PS reference clock 100MHz/3 ($33.\overline{3}$MHz), 1.8V LVCMOS
- GTR_CLK0: USB 3.0 26MHz, LVDS
- GTR_CLK1: DisplayPort 27MHz, LVDS

The clocking architecture on Ultra96-V2 uses a programmable IDT - Integrated Device Technology, Inc. VersaClock® 6E:

https://www.idt.com/us/en/products/clocks-timing/clock-generation/programmable-clocks/5p49v6975-programmable-versaclock-clock-generator-integrated-crystal

In the block diagram below, you can see the various differential (LVDS) and single-ended (SE) clock outputs from that Avnet programmed into our VersaClock design.

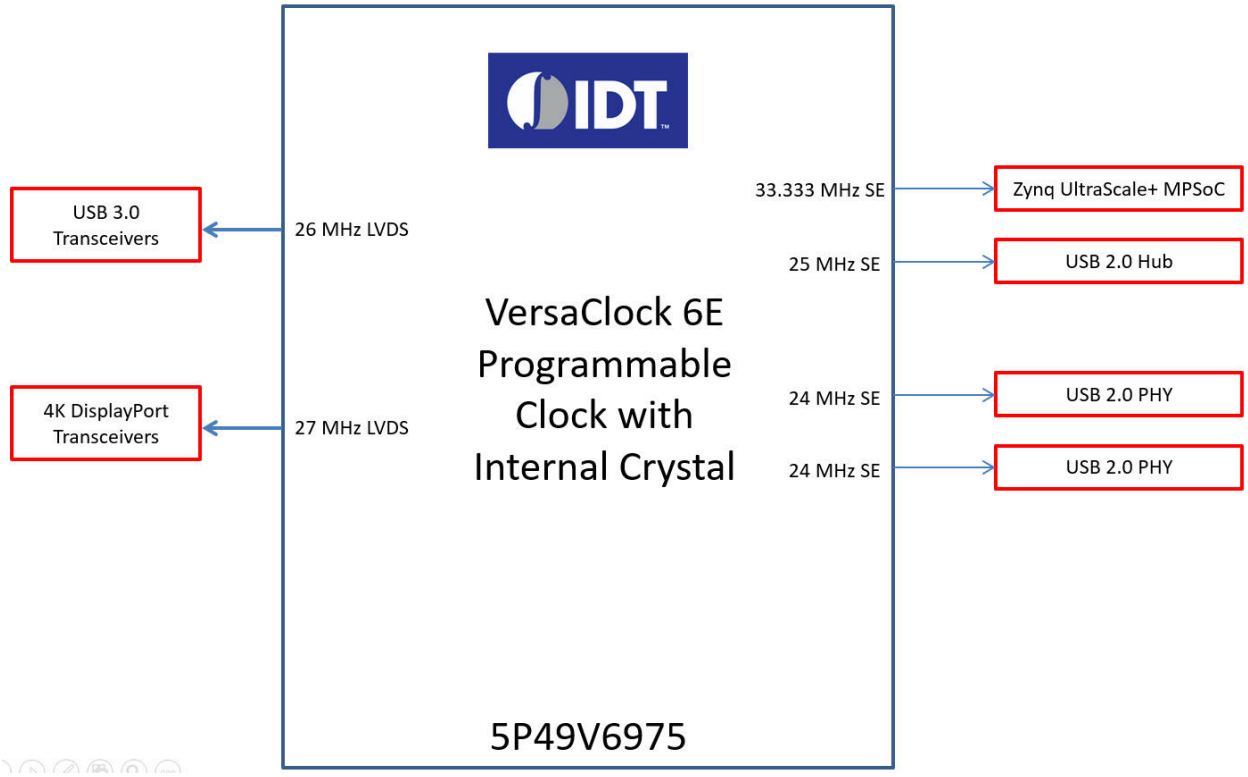


Figure 7 – Ultra96-V2 Clock Architecture

Benefits made possible on the Ultra96-V2 with the IDT VersaClock 6E

- Eliminated external crystal
- Replaced a clock synthesizer and 3 external oscillators with a single VersaClock
- Made use of two differential and four single-ended outputs at five different frequencies
- Programmed multiple configurations to give us the flexibility for other design scenarios without reprogramming or replacing the chip
- Met all our performance requirements for USB 3.0, USB 2.0, DisplayPort, and the Xilinx MPSoC primary clock input.

Avnet's TCS file or datasheet addendum for this clock chip may be requested from your Avnet FAE or by filling out the survey at http://Avnet.me/AvnetProgrammingFiles. The custom, pre-programmed part number for the Ultra96-V2 Programmable Clock is 5P49V6975A114LTGI, which is available at https://www.avnet.com/shop/us/products/renesas-electronics/5p49v6975a114ltgi-3074457345638736880

Table 21 – Clock Generator Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	MPSoC VCCO	Function	Connects to:		Connects to:	
						REFDES	REFDES Pin Number	REFDES	REFDES Pin Number
H14	503	PS_REF_CLK_503	PS_REF_CLK	+VCC_PSAUX = 1.8V	System Reference Clock	U5	14	N/A	N/A
J20	505	PS_MGTREFCLK1N_505	U27M_N	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Clock Reference	U5	16	N/A	N/A
J19	505	PS_MGTREFCLK1P_505	U27M_P	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	DisplayPort Clock Reference	U5	17	N/A	N/A
L20	505	PS_MGTREFCLK0N_505	U26M_N	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	USB 3.0 Clock Reference	U5	19	N/A	N/A
L19	505	PS_MGTREFCLK0P_505	U26M_P	+MGTRAVCC = 0.85V +MGTRAVTT = 1.8V	USB 3.0 Clock Reference	U5	20	N/A	N/A
N/A	N/A	N/A	USB_HUB_25MHz	N/A	USB 3.1 Hub Clock Reference	U5	24	U16	54
N/A	N/A	N/A	USB_CLKB	N/A	USB 2.0 PHY Clock Reference	U5	11	U4	26
N/A	N/A	N/A	USB_CLKA	N/A	USB 2.0 PHY Clock Reference	U5	12	U14	26
N/A	N/A	N/A	TP23	N/A	test point	U5	13	TP23	1

5.11 On/Off Controller

The Xilinx Zynq UltraScale+ MPSoC device has an integrated Platform Management Unit or PMU. This PMU's functionality is described in Chapter 6 of Xilinx UG1085, *Zynq UltraScale+ Device Technical Reference Manual.* The PMU controls many things on the ZU+ device, including powering up and down the ZU+. The Ultra96-V2 incorporates an On/Off controller to interface between the on-board power regulators and the ZU+. This allows the ZU+, Power Button, and regulators to seamlessly work together to power the system on and off without corrupting your Linux (or other OS) file system.

The key inputs/outputs of the system are detailed below:

Table 22 – On/Off Controller Inputs and Outputs

Signal Name	Source	Destination	Polarity	Description
PWR_PB_N	Push Button (SW4)	On/Off Controller (U6)	Low-enabled	Push button input for powering on and off. Responds to both short and long pushes. When the system is powered off, a short or long push initiates a power-on sequence. When the system is powered on, a short push will trigger an interrupt, telling the Xilinx PMU to perform a shutdown. A long push (~10 seconds held down) will also issue an interrupt but will power off the system regardless of whether the PMU issues KILL_N or not.
MIO34_POWER_KILL_N	ZU+ (U1)	On/Off Controller (U6)	Low-enabled	Disable the power regulators immediately. The ZU+ PMU enables this when it has properly processed an internal shutdown command successfully and is ready for the on/off controller to turn off the regulators.
EN_SEQ_PL	On/Off Controller (U6)	Pmics (U11, U12, U21)	High-enabled	Enables the three primary Infineon power regulation devices. Asserted by the On/Off Controller during a power-up sequence, and de-asserted by the On/Off Controller during a power-down sequence (either a response to KILL_N or a long push).
MIO26_PWR_INT	On/Off Controller (U6)	ZU+ (U1)	High-enabled	Interrupt input to the ZU+ when a power-down push button event has been received.
INIT	Strapping resistor (JT6)	On/Off Controller (U6)	Default = Low	When low, the On/Off Controller powers up with the push button control. When high, the On/Off Controller powers up the system as soon as the input voltage is valid.

The Ultra96-V1 used an off-the-shelf On/Off Controller, but it had a couple deficiencies:

- No capability to turn on immediately when Power is applied. An option to be able to do this is a requirement of the 96Boards Spec. To do this on Ultra96-V1 required soldering multiple components and bypassing the On/Off Controller.

- Interrupt polarity was low while the Xilinx PMU requires high

A Dialog Semiconductor GreenPAK programmable device was developed to accomplish this function on Ultra96-V2. This device accomplishes everything needed in a very small 2mm x 2.2mm STQFN package. Specifically, the design is based on the Dialog GreenPAK SLG46170 device, with the programmed part number being SLG4G42480V. If you want to duplicate the exact functionality of the On/Off Controller on the Ultra96-V2, the SLG4G42480V may be ordered from Avnet. If you are working on a project with Avnet as your distributor, work with your Avnet FAE to request samples of the device to avoid the 3K MOQ, or you can get Avnet's code for the On/Off Controller to customize it for yourself by submitting a request at http://Avnet.me/AvnetProgrammingFiles.

For those that want to modify the power-up initialization from push-button control to power-up with power connected, you will need to move a single resistor on the Ultra96-V2. This is the 3-pad, 10-Kohm resistor JT6, which selects either pull-down (default, use Push Button) or pull-up (power up with power). To implement the ***Power Up with Power Connected*** function, move the JT6 from position 1-2 to position 2-3. JT6 is located on the backside of the Ultra96-V2, so you will first need to remove the heatsink. JT6 is then located in the upper right of the southwest quadrant, near U6 as highlighted in the photo below.

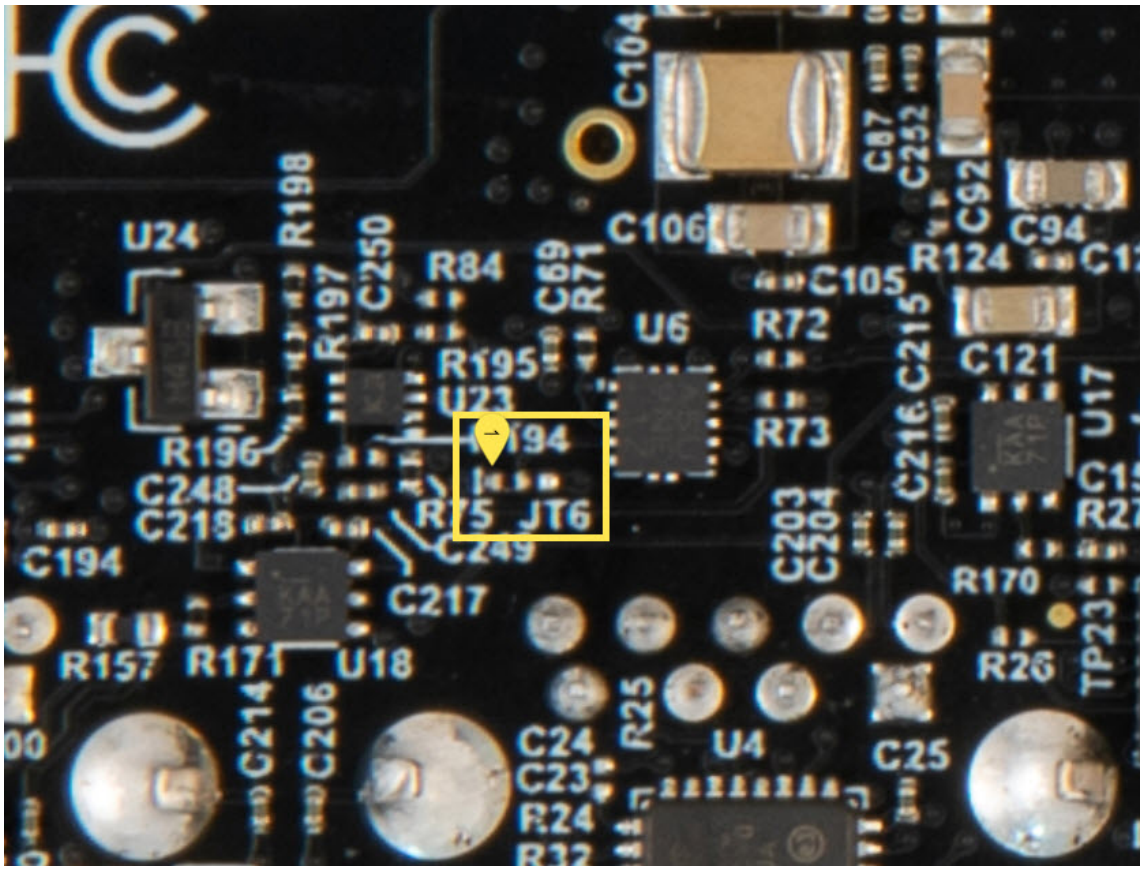


Figure 8 – Location of JT6

To help explain the functionality of this device, a datasheet is available at Dialog SLG4G42480 On-Off Controller Datasheet . Also, here are several functional diagrams showing the logic within this device.

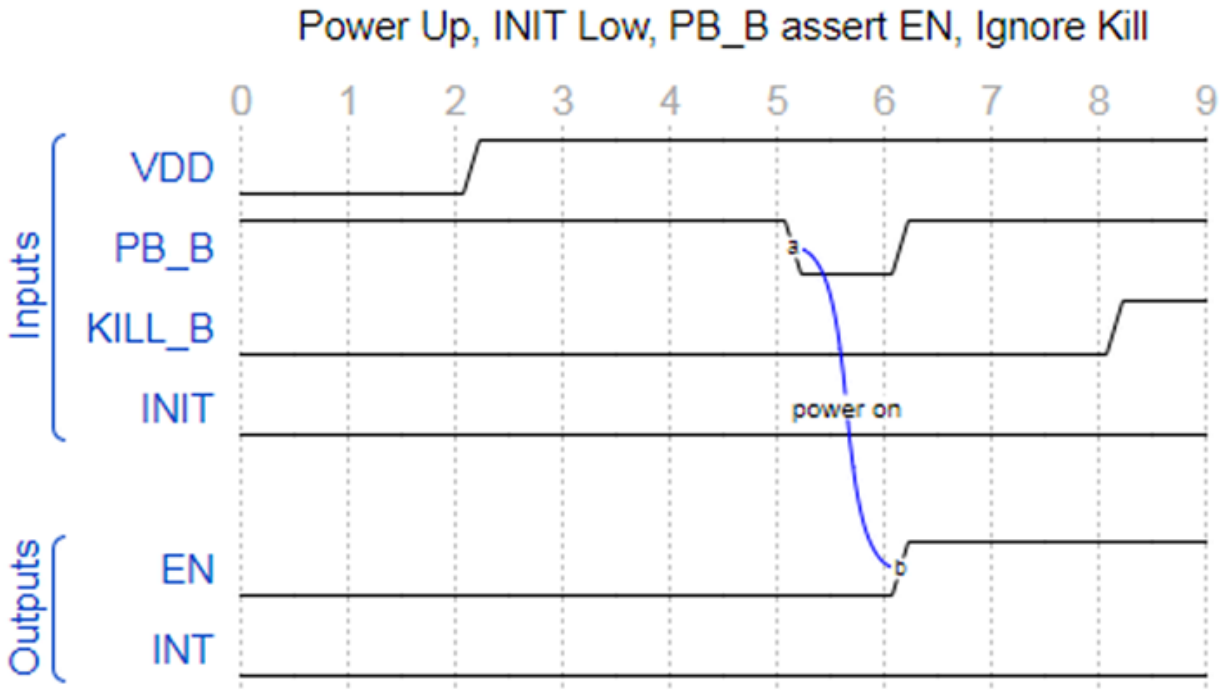


Figure 9 – On/Off Controller Diagram 1

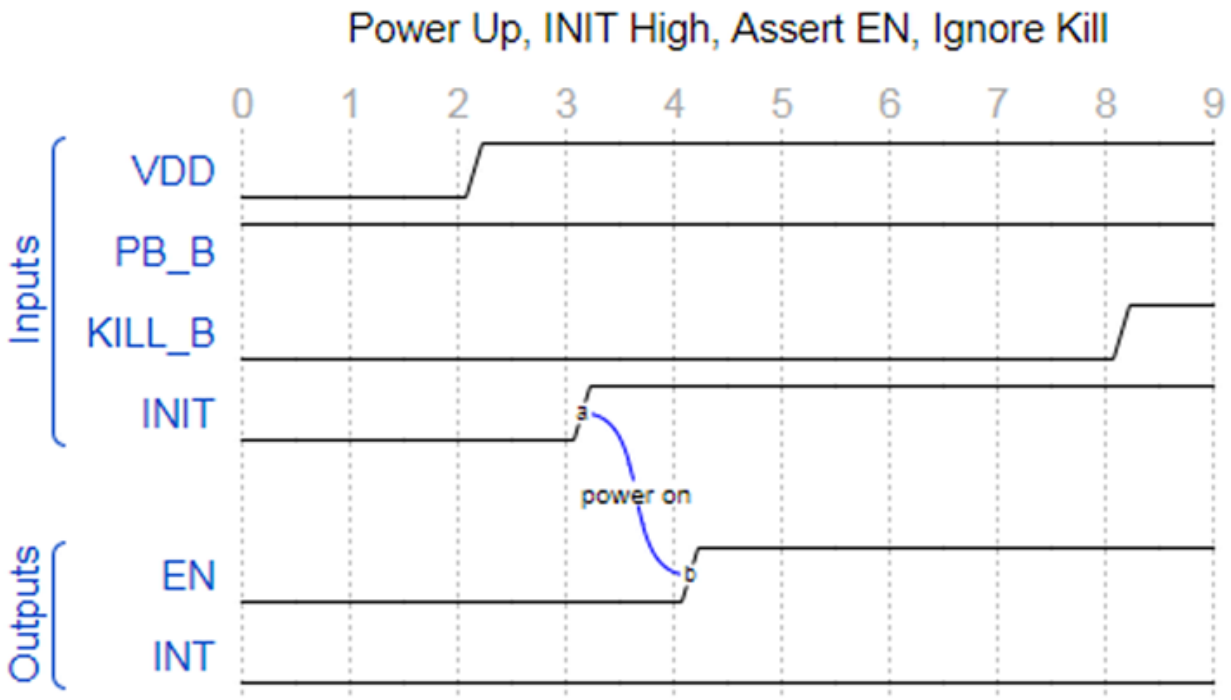


Figure 10 – On/Off Controller Diagram 2

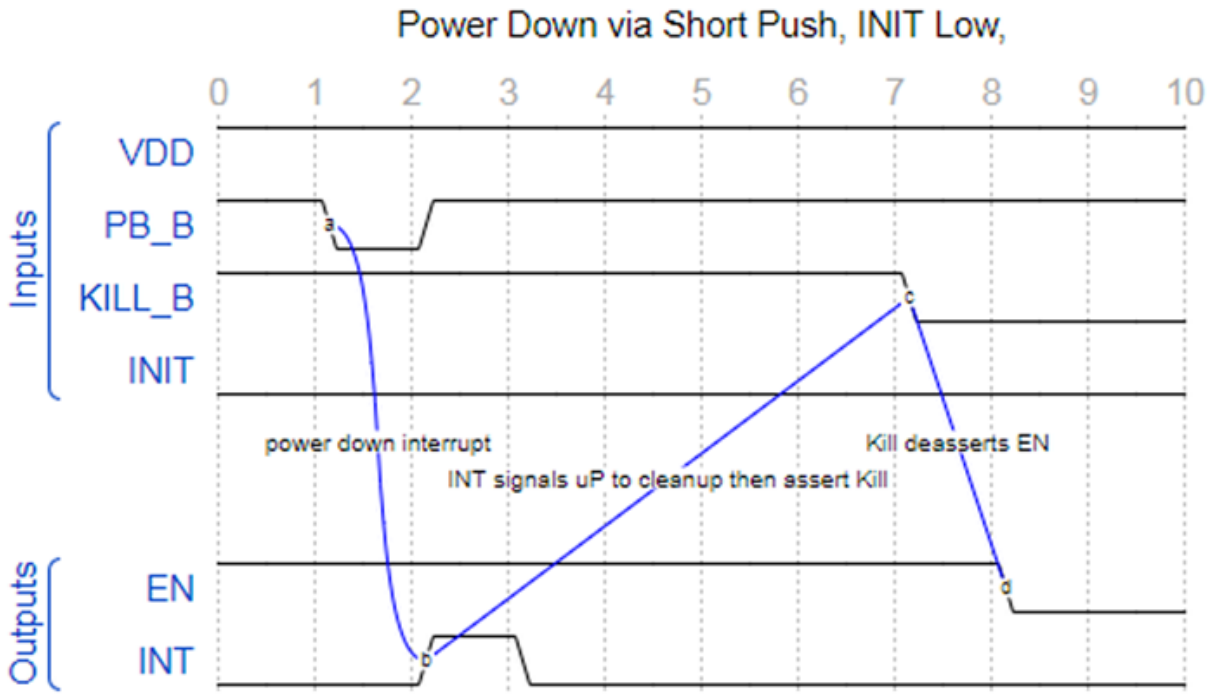


Figure 11 – On/Off Controller Diagram 3

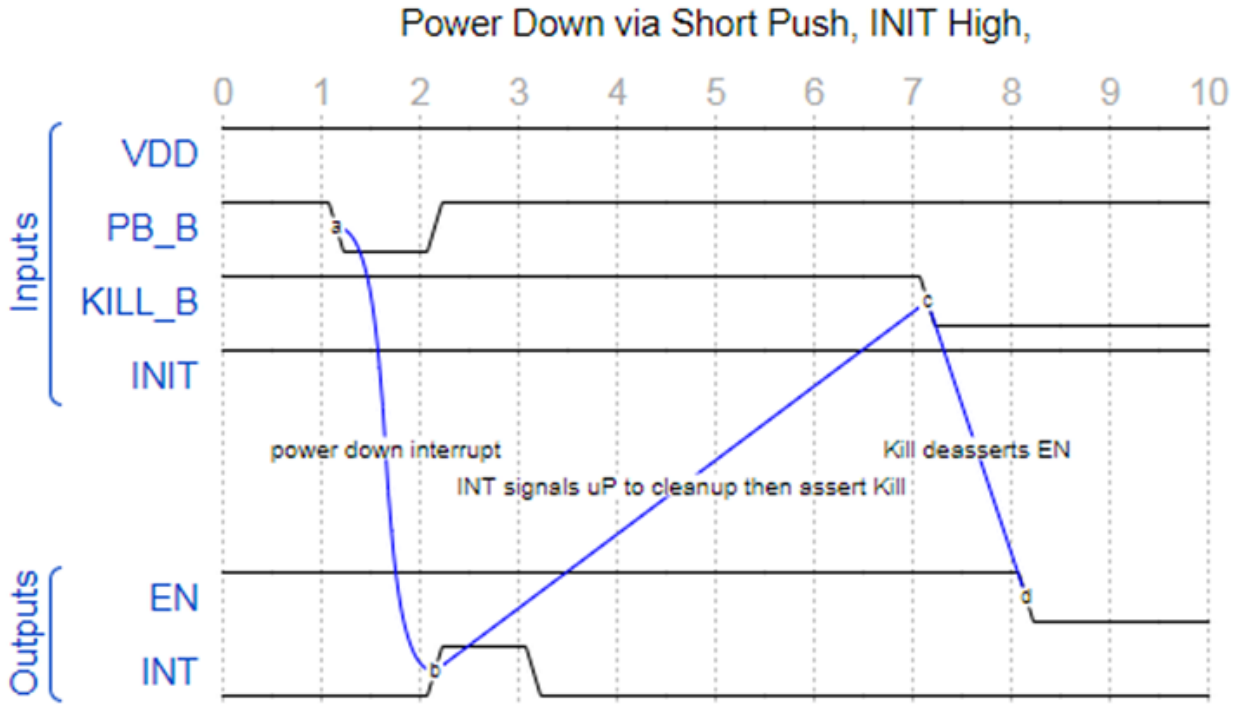


Figure 12 – On/Off Controller Diagram 4

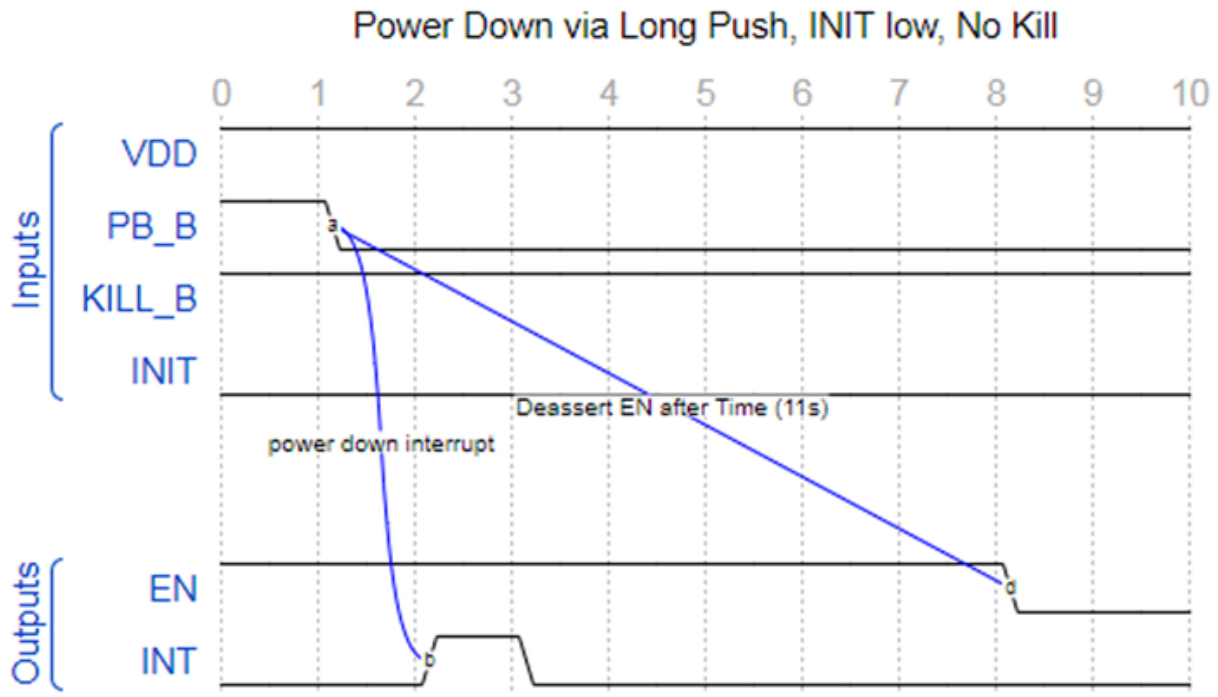


Figure 13 – On/Off Controller Diagram 5

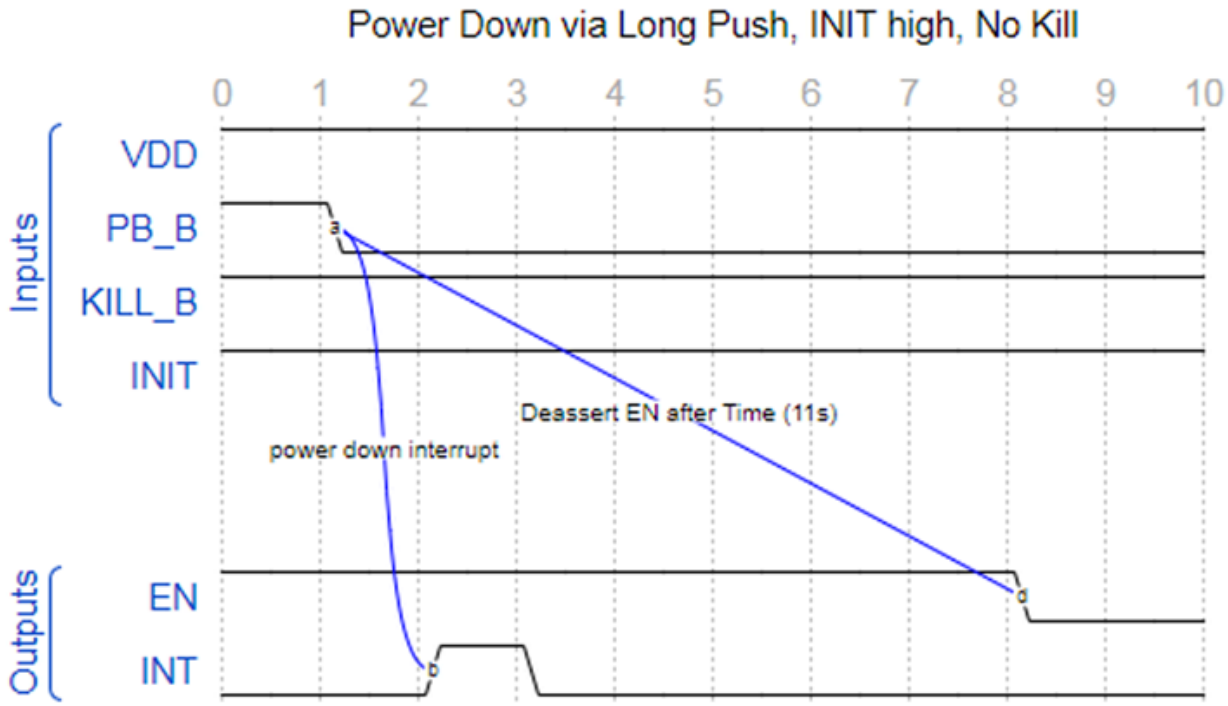


Figure 14 – On/Off Controller Diagram 6

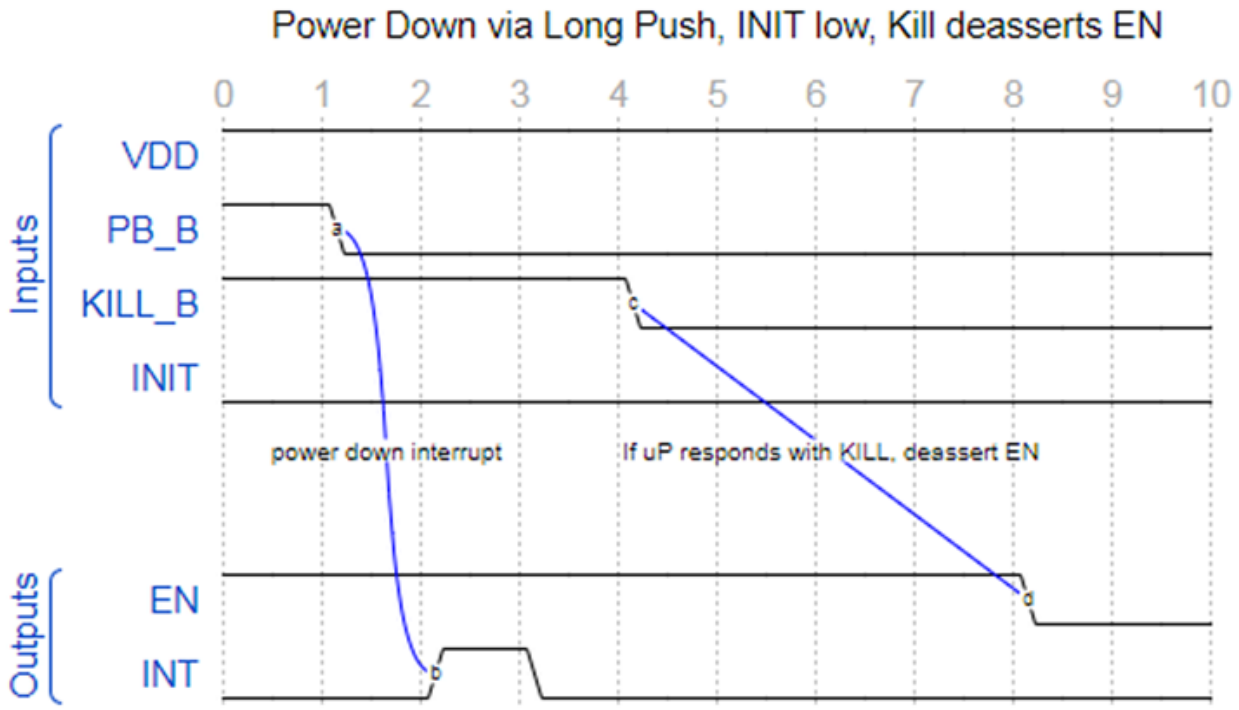


Figure 15 – On/Off Controller Diagram 7

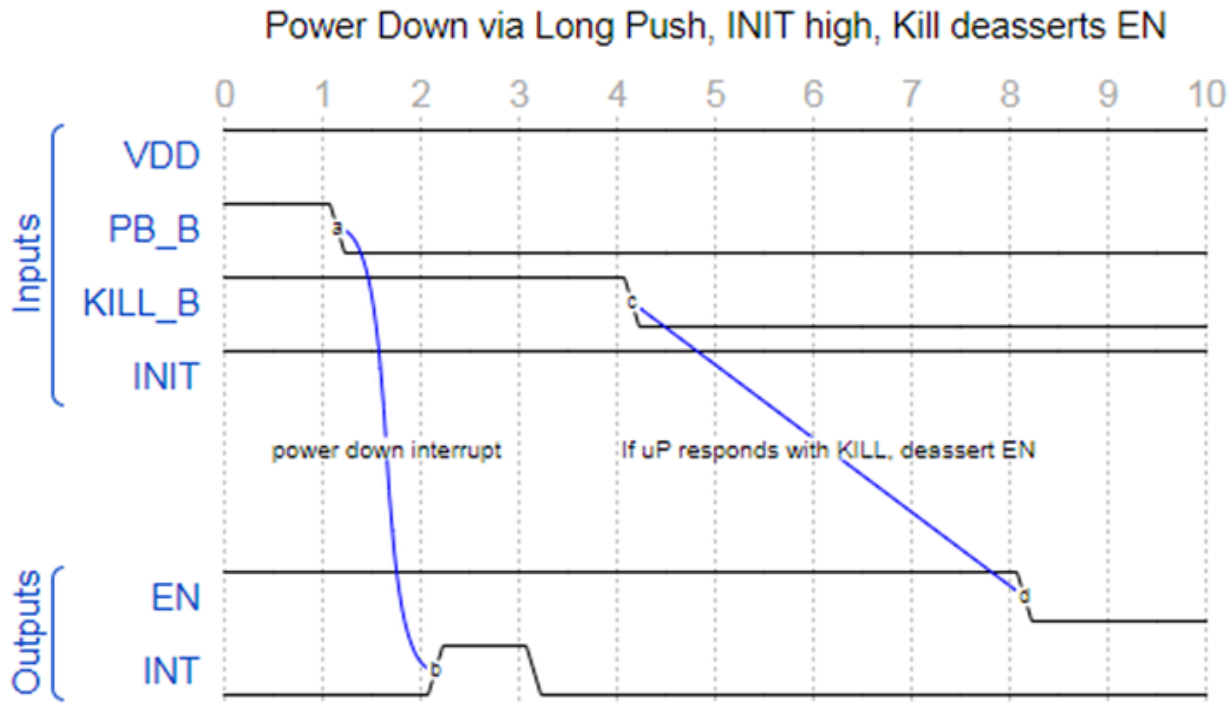


Figure 16 – On/Off Controller Diagram 8

Table 23 – On/Off Controller Pin Table

MPSoC Pin Number	Bank	MPSoC Site Name	Ultra96-V2 Net name	MPSoC VCCO	Function	Connects to:	
						REFDES	REFDES Pin Number
G9	501	PS_MIO26_501	MIO26_PWR_INT	+VCC_PSAUX = 1.8V	On/Off Controller	U6	11
F13	501	PS_MIO34_501	MIO34_POWER_KILL_N	+VCC_PSAUX = 1.8V	On/Off Controller	U6	10

5.12 Expansion Connectors

5.12.1 Low Speed Expansion Connector (J5)

Ultra96-V2 provides a 96Boards compatible Low Speed Expansion Connector. A Molex 87381-4063 (or compatible) 40 pin low profile female 2mm receptacle (20x2) 4.5mm height is specified.

Table 24 shows the pinout of the Low Speed Expansion Header (Ultra96-V2 column) and the differences from the 96Boards specification (96Boards column). Except for I2C0 and I2C1, all dedicated interfaces specified by 96Boards can be replaced with GPIO or any other IP supported by Zynq UltraScale+.

Table 24 – Low Speed Expansion Connector (J5)

Ultra96	96Boards	Pin #		Pin #	96Boards	Ultra96
GND	GND	1		2	GND	GND
HD_GPIO0	UART0_CTS	3		4	PWR_BTN_N	PWR_BTN_N
HD_GPIO1	UART0_TxD	5		6	RST_BTN_N	RST_BTN_N
HD_GPIO2	UART0_RxD	7		8	SPI0_SCLK	PS_MIO38
HD_GPIO3	UART0_RTS	9		10	SPI0_DIN	PS_MIO42
HD_GPIO4	UART1_TxD	11		12	SPI0_CS	PS_MIO41
HD_GPIO5	UART1_RxD	13		14	SPI0_DOUT	PS_MIO43
PS_I2C0_SCL	I2C0_SCL	15		16	PCM_FS	HD_GPIO9
PS_I2C0_SDA	I2C0_SDA	17		18	PCM_CLK	HD_GPIO10
PS_I2C1_SCL	I2C1_SCL	19		20	PCM_DO	HD_GPIO11
PS_I2C1_SDA	I2C1_SDA	21		22	PCM_DI	HD_GPIO12
PS_MIO36	GPIO-A	23		24	GPIO-B	PS_MIO37
PS_MIO39	GPIO-C	25		26	GPIO-D	PS_MIO40
PS_MIO44	GPIO-E	27		28	GPIO-F	PS_MIO45
HD_GPIO6	GPIO-G	29		30	GPIO-H	HD_GPIO13
HD_GPIO7	GPIO-I	31		32	GPIO-J	HD_GPIO14
HD_GPIO8	GPIO-K	33		34	GPIO-L	HD_GPIO15
+1V8	+1V8	35		36	SYS_DCIN	SYS_DCIN
+5V0	+5V0	37		38	SYS_DCIN	SYS_DCIN
GND	GND	39		40	GND	GND

5.12.2 High Speed Expansion Connector (J4)

Ultra96-V2 provides a 96Boards compatible High-Speed Expansion Connector. An Amphenol FCI 61082-061409LF (or compatible) 60 pin low profile 0.8mm receptacle is specified.

Table 25 shows the pinout of the High-Speed Expansion Header (Ultra96-V2 column) and the differences from the 96Boards specification (96Boards column). Except for SD, I2C2 and I2C3, all dedicated interfaces specified by 96Boards may be replaced with GPIO or any other IP supported by Zynq UltraScale+. All P/N signals are routed as differential pairs (14 pairs total).

Table 25 – High Speed Expansion Connector

Ultra96	96Boards	Pin #	Pin #	96Boards	Ultra96
MIO11_SPI1_MOSI	SD_DAT0/SPI1_DOUT	1	2	CSI0_C+	CSI0_C_P
n/c	SD_DAT1	3	4	CSI0_C-	CSI0_C_N
n/c	SD_DAT2	5	6	GND	GND
MIO9_SPI1_CS	SD_DAT3/SPI1_CS	7	8	CSI0_D0+	CSI0_D0_P
MIO6_SPI1_SCLK	SD_SCLK/SPI1_SCLK	9	10	CSI0+D0-	CSI0_D0_N
MIO10_SPI1_MISO	SD_CMD/SPI1_DIN	11	12	GND	GND
GND	GND	13	14	CSI0_D1+	CSI0_D1_P
CSI0_MCLK	CLK0/CSI0_MCLK	15	16	CSI0_D1-	CSI0_D1_N
CSI1_MCLK	CLK1/CSI1_MCLK	17	18	GND	GND
GND	GND	19	20	CSI0_D2+	CSI0_D2_P
DSI_CLK_P	DSI_CLK+	21	22	CSI0_D2-	CSI0_D2_N
DSI_CLK_N	DSI_CLK-	23	24	GND	GND
GND	GND	25	26	CSI0_D3+	CSI0_D3_P
DSI_D0_P	DSI_D0+	27	28	CSI0_D3-	CSI0_D3_N
DSI_D0_N	DSI_D0-	29	30	GND	GND
GND	GND	31	32	I2C2_SCL	HSEXP_I2C2_SCL
DSI_D1_P	DSI_D1+	33	34	I2C2_SDA	HSEXP_I2C2_SDA
DSI_D1_N	DSI_D1-	35	36	I2C3_SCL	HSEXP_I2C3_SCL
GND	GND	37	38	I2C3_SDA	HSEXP_I2C3_SDA
DSI_D2_P	DSI_D2+	39	40	GND	GND
DSI_D2_N	DSI_D2-	41	42	CSI1_D0+	CSI1_D0_P
GND	GND	43	44	CSI1_D0-	CSI1_D0_N
DSI_D3_P	DSI_D3+	45	46	GND	GND
DSI_D3_N	DSI_D3-	47	48	CSI1_D1+	CSI1_D1_P
GND	GND	49	50	CSI1_D1-	CSI1_D1_N
USB2D3_P	USB_D+	51	52	GND	GND
USB2D3_N	USB_D-	53	54	CSI1_C+	CSI1_C_P
GND	GND	55	56	CSI1_C-	CSI1_C_N
HSIC_STR	HSIC_STR	57	58	GND	GND
HSIC_DATA	HSIC_DATA	59	60	Reserved	100K-ohm Pull-up

6 Configuration and Debug

6.1 Boot Mode

Ultra96-V2 supports booting from JTAG and microSD Card. A DIP switch (SW3) is installed to allow selecting the desired boot mode.

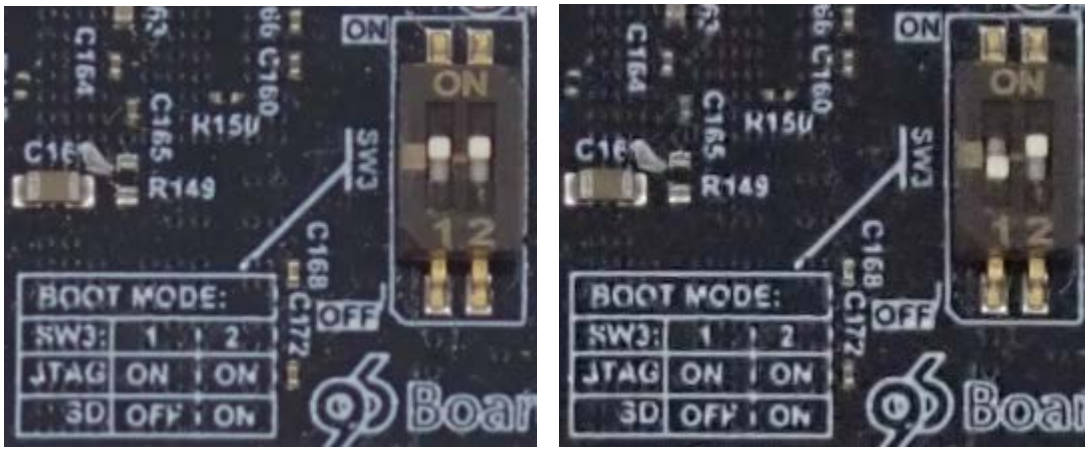


Figure 17 – Boot Mode Switch (JTAG Boot on Left, SD Card Boot on Right)

6.2 JTAG Configuration and Debug

JTAG access to the MPSoC is available through a 1x8 header (J3). The Avnet JTAG/UART Pod (AES-ACC-U96-JTAG) can directly interface with the 1x8 Ultra96-V2 header and is available for purchase as an accessory.

http://avnet.me/ultra96jtag

Other JTAG modules can be used with flyleads, although using 0.1” to 2mm wire leads is recommended.

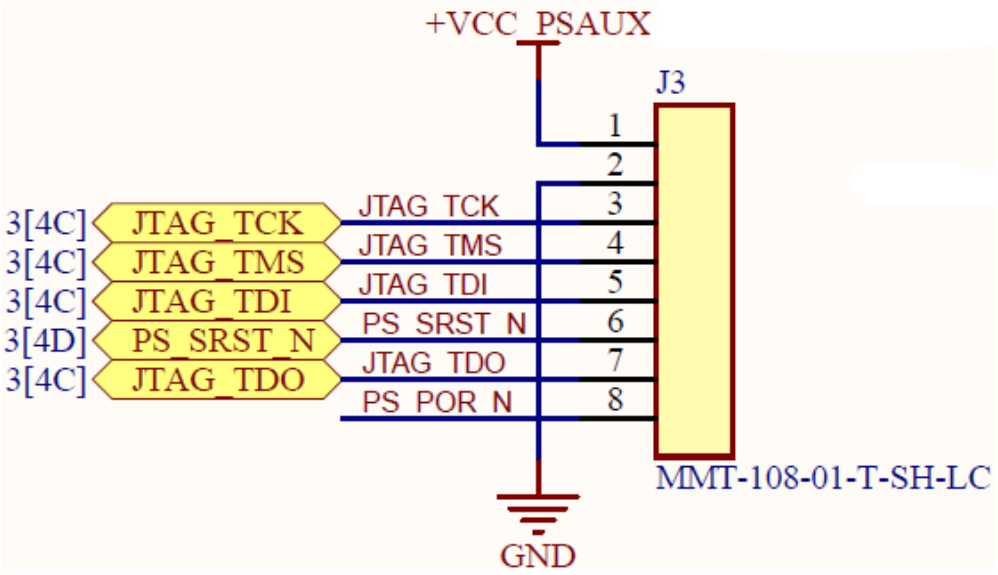


Figure 18 – Ultra96-V2 JTAG Connection

7 Power

7.1 External Power Connections

Board power may be supplied three different ways to the Ultra96-V2

1. 96Boards compliant barrel jack (J10)
2. Two-pin header (JP1) – not populated by default
    a. D20 must also be populated or shorted before using this path
3. Low-Speed Mezzanine Pins 36 and 38

Because of the opportunity to have multiple sources driving the same input, protection diodes are in place (D19 for barrel jack, D20 for JP1, and D18 for LS Mezzanine).

7.1.1 Mezzanine Power

The 96Boards specification allows the LS Mezzanine to either receive or supply system power. The Ultra96-V2 is set up to allow the LS Mezzanine to deliver power to the Ultra96-V2 main board. This requires the power source at the Mezzanine.

If you want to supply Mezzanine power from the Ultra96-V2 to the Mezzanine, then you must either reverse or short protection diode D18, after which you should use extreme care to be careful that you do not simultaneous apply power at both the barrel jack and mezzanine.

7.1.2 Barrel Jack

The most common way to power Ultra96-V2 is through the barrel jack, which is supplied by an external 12V AC/DC Power Supply based on the 96Boards specification, located at https://www.96boards.org/product/power/.

Here are the requirements from the 96Boards site:

EIAJ-3 compliant DC plug available up to 2A, which is 4.75 mm outer diameter with 1.7mm center pin (4.75/1.7), for the power supply

https://en.wikipedia.org/wiki/EIAJ_connector

Avnet offers a 12V supply as an accessory (part number: AES-ACC-U96-4APWR) available at http://avnet.me/96BoardPower4A and http://avnet.me/96BoardPower4A-E14, with the following specifications:

- Input: 100-240V, 50/60HZ
- US Plug 12V 4A power adapter
- 1.2m DC cable with ferrite
- 4.7mm * 1.7mm * 10 mm dc plug, Level VI
- International plugs

Figure 19 – Ultra96-V2 12V @ 2A AC/DC Supply

7.2 Power Estimation Using XPE

Xilinx Power Estimator (XPE) should be used to generate worst case power estimations. The Xilinx Power Estimator (XPE) spreadsheet is available on Xilinx' website that can help you get started with your own power estimation. Avnet has also provided an example of this spreadsheet filled out for the Ultra96-V2 under Documentation on the Ultra96-V2 website.

http://avnet.me/ultra96-v2 → Technical Documents → Power Analysis

This blog also gives some good information about using XPE.

https://www.element14.com/community/groups/power-management/blog/2018/01/11/estimating-xilinx-power-requirements

7.3 Power Regulators

A configurable multi-rail PMIC provides all power for the Ultra96-V2. The power rail configuration is shown below:

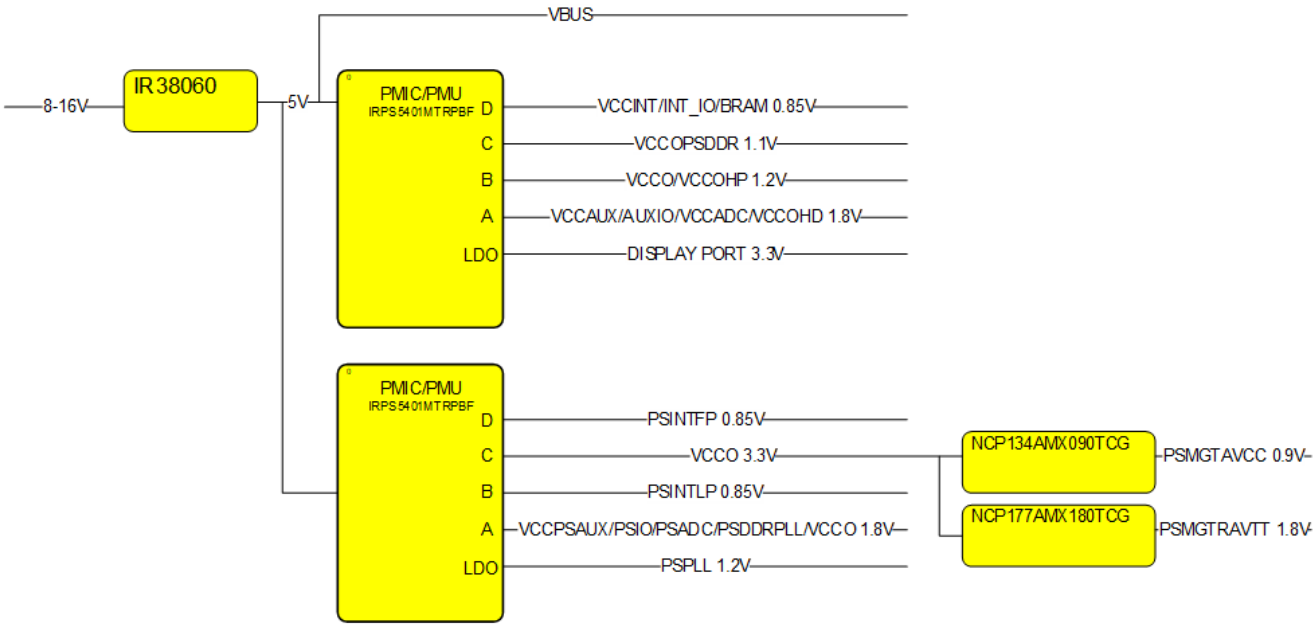


Figure 20 – Ultra96-V2 DC-DC Power Regulation

7.4 Power Sequence

The diagram below shows the power sequence:

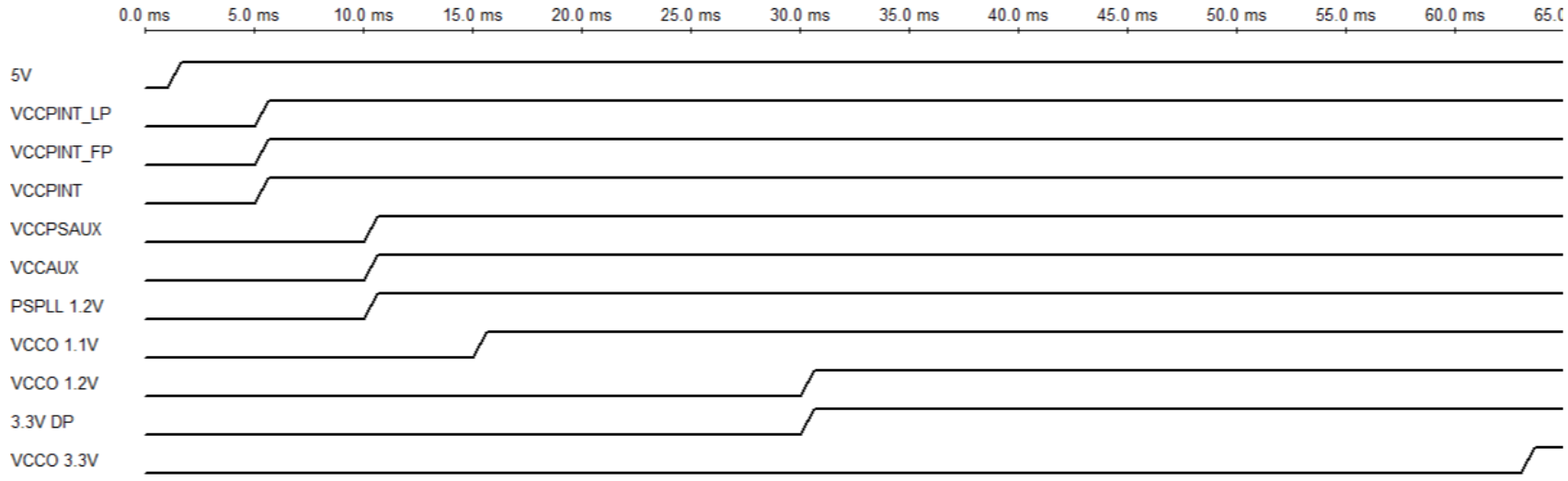
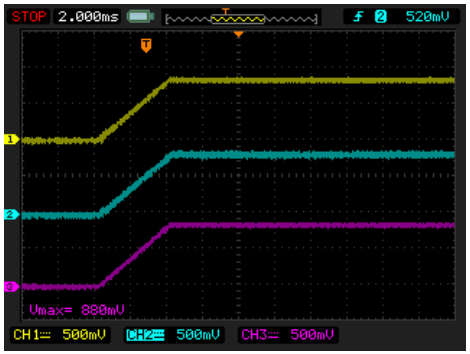


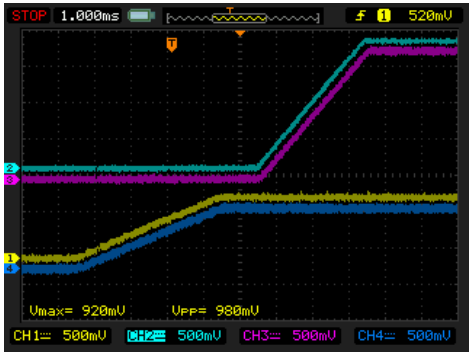
Figure 21 – Ultra96-V2 Power Sequencing

The captures below show the power up sequencing measurements taken on the Ultra96-V2:

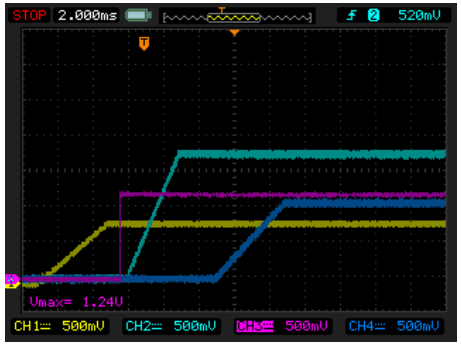
Pink – 5V
Yellow – VCCPSINT_LP
Light Blue – VCCPSAUX
Dark Blue – VCCO PSDDR 1.1V



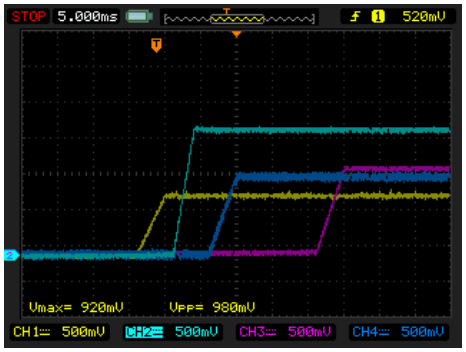
Yellow – VCCPSINT_LP
Blue – VCCPSINT_FP
Pink – VCCINT



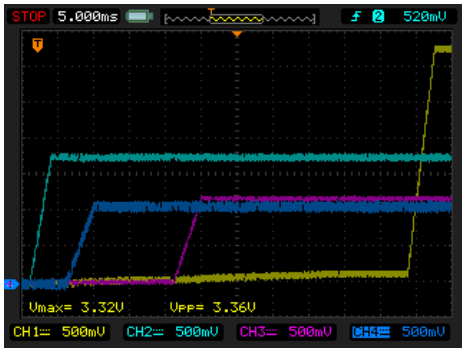
Yellow – VCCPSINT_LP
Dark Blue – VCCINT
Light Blue – VCCPSAUX
Pink – VCCAUX



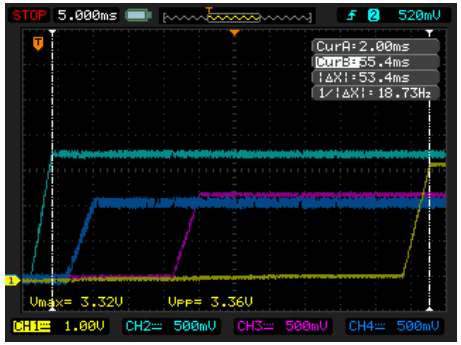
Yellow – VCCPSINT_LP
Pink – PSPLL
Light Blue – VCCPSAUX
Dark Blue – VCCO PSDDR 1.1V



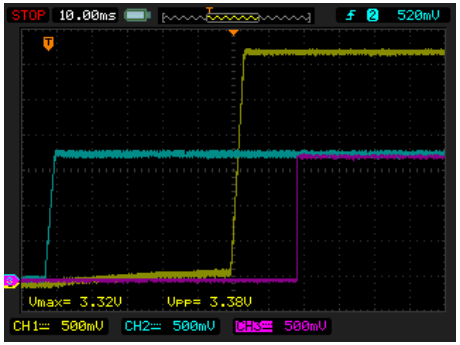
Yellow – VCCPSINT_LP
Light Blue – VCCPSAUX
Dark Blue – VCCO PSDDR 1.1V
Pink – VCCO 1.2V



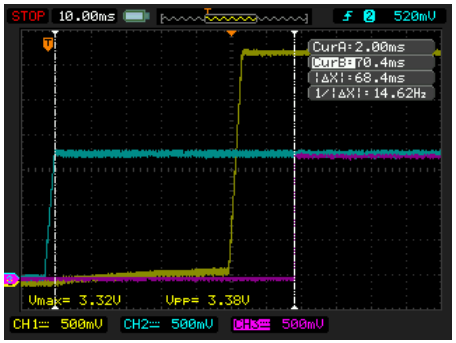
Light Blue – VCCAUX
Dark Blue – VCCO PSDDR 1.1V
Pink – VCCO 1.2V
Yellow – 3.3V



Timing VCCAUX to 3.3V – 53ms



Light Blue – VCCAUX
Yellow – 3.3V
Pink – POR



68ms from VCCAUX to POR (65ms required)

8 Thermal

The Ultra96-V2 is designed with mounting holes to attach a device to help dissipate heat. Two different devices have shipped with Ultra96-V2, as shown below. Both devices also have additional mounting holes to secure them to an enclosure.

- Rev 1, datecodes 1935 and earlier (C-grade only): Mounted on thermal bracket with fan
  - Custom bracket
  - Sunon MF30060V1-1000U-A99 fan (Connect to 5V and GND at TP25 and TP26)
    - Users can control the fan using signal FAN_PWM from PL IO F4 on Bank 65.
- Rev 1, datecodes 1936 and later (C- and I-grades): Custom Aavid passive heatsink
- Rev 2 (C- and I-grades): Custom Aavid passive heatsink

8.1 External Airflow

The Aavid Heatsink does not have an attached fan. It is passive. The heatsink spans the entire board and is extremely efficient at pulling heat away from the entire board -- especially the ZU+ MPSoC and the three Pmics. When we initially experimented with this board on a benchtop with a few moderately intensive designs, the heatsink did not get hot to the touch even without airflow. However, when we tested the I-grade design at +85C in the thermal chamber, we implemented airflow within the chamber at a rate of 6.8 m/sec. While running a design that was very intensive in PL usage and Clock Frequency, we used the Vivado HW manager to ensure the MPSoC T_j did not exceed 97C, which gave us a few degrees margin compared to the 100C T_j specification.

Given the flexibility of the Xilinx ZU+ PL, every design is different and must be analyzed once the final application is developed. When Ultra96-V2 is mounted in an enclosure or used in a system design, it is expected that the system designer account for an appropriate amount of system-level airflow that keeps the MPSoC T_j within the bounds of the device.

While you should typically not have any issues running Ultra96-V2 on a bench with the new heatsink without airflow, this may not always be the case. If you run a PL- and Clock-intensive design, you may see the heatsink temperature rise 20 or 30 degrees above ambient. You will not want to touch the heatsink at this temperature. You should use caution and perhaps apply a small desktop fan which will bring the heatsink back within 5 to 10 degrees of ambient.

You may also choose to wire a fan into the Ultra96-V2 as the board still provides access to a DC voltage to run a fan (controlled by signal FAN_PWM, default = 5V with 3.3V and Vin options. See Sheet 9 of Schematics). Please see this blog for more information.

https://www.element14.com/community/groups/power-management/blog/2020/10/23/upgrading-ultra96-v2-to-the-passive-heatsink-how-to

8.2 Mounting the Ultra96-V2

Both the bracket/fan assembly and the new Aavid heatsink have mounting options so the Ultra96-V2 can be secured to a bulkhead. However, note that the screw size on the Aavid heatsink is different than the previous bracket/fan.

Heat dissipation	PCB Mount	Enclosure/Bulkhead Mount
Ultra96-V1 and -V2 bracket fan	4x M2.5 x 8mm screw (included)	4x #4-40 screw (not included, length based on application)
Ultra96-V2 Aavid heatsink	4x M2.5 x 8mm screw (included)	4x M2.5 screw (not included, length based on application)

9 Reset

The Ultra96-V2 System Reset is managed by signal POWER_GOOD, which is an open-drain signal, which is pulled-up to +VCC_PSAUX (+1.8V) through 49.9KΩ R116. This signal is tied to the MPSoC Power-on-Reset signal PS_POR_B. There are multiple entities that can assert this signal by driving low:

- Infineon PMICs (U11, U12, U21)
- Pushbutton Reset (SW2)
- Low-Speed Expansion Connector (J5) Pin 6

At power-up, the ZU3EG is held in reset by the PMICs until all power rails have ramped up and are stable. A Low-Speed Mezzanine may also choose to hold the system in Reset to allow initialization of any mezzanine circuitry. A pushbutton (SW2) allows manually resetting the ZU3EG.

10 Specifications and Ratings

This section contains the absolute maximum and the recommended operating ranges for SBC temperature, supply voltages, and I/O voltages. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

10.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes	Reference Document
Storage Temperature	-40	85	°C		

Table 38 – Absolute Maximum Temperature Rating

Parameter	Min	Max	Units	Notes	Reference Document
+VSYS_IN	-0.3	24.0	V		NCP716MT33 Datasheet IRPS38060M Datasheet

Table 39 – Absolute Maximum Ratings for Input Supply Voltage

10.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
C-Grade SBC	0	70	°C	Zynq UltraScale+ Tj < 100°C Micron LPDDR4 Tc < 95°C USB3320 Tj < 100°C IRPS5401 Tj < 125°C IRPS38060M Tj < 125°C	Xilinx Datasheet DS925 Micron Datasheet Microchip Datasheet USB3320 IRPS5401 Datasheet IRPS38060M Datasheet
I-Grade SBC	-40[1]	85	°C	Zynq UltraScale+ Tj < 100°C Micron DDR4 Tc < 95°C[2] USB3320 Tj < 100°C. IRPS5401 Tj < 125°C IRPS38060M Tj < 125°C	

Table 41 – Recommended Ambient Operating Temperature

There are two exceptions to the -40C rating on the Ultra96-V2 I-grade, which are:

- J2, TE Connectivity microSD Card Cage, 2201778-1 (rated -30C to +85C) See https://www.te.com/usa-en/product-2201778-1.datasheet.pdf
- J10, CUI Barrel Jack, PJ1-021-SMT-TR (rated -25C to +85C) See https://www.cuidevices.com/product/resource/pj1-021-smt-tr.pdf

Both devices have spring-type mechanisms inside them that can become brittle at very cold temperatures. If the mechanism is exercised at extremely cold temperatures, the mechanism could break. Avnet did test the Ultra96-V2 to the full -40C temperature; however, we did not insert/remove either the power jack or microSD card at -40C. These items were inserted at room temperature, after which the entire Device Under Test was placed in a thermal chamber and then soaked to -40C. Under these conditions, the board passed all testing, and the hardware was not damaged.

If you need an Ultra96-V2 where the power jack or microSD card must be removed or inserted at -40C, Avnet has researched options that will work, but it requires small modifications to the PCB. If this is something you are interested in pursuing, please discuss with your local Avnet FAE or contact customize@avnet.com.

[1] There are two exceptions to the -40C rating on the Ultra96-V2 I-grade, which are:
J2, TE Connectivity microSD Card Cage, 2201778-1 (rated -30C to +85C)
See https://www.te.com/usa-en/product-2201778-1.datasheet.pdf
J10, CUI Barrel Jack, PJ1-021-SMT-TR (rated -25C to +85C)
See https://www.cuidevices.com/product/resource/pj1-021-smt-tr.pdf

[2] Enable temperature-controlled refresh mode if T_c exceeds 85°C.

Parameter	Min	Max	Units	Notes	Reference Document
+VSYS_IN	7.0	14.0	V		NCP716MT33 Datasheet IRPS38060M Datasheet

Table 42 – Recommended Supply Voltage

11 Getting Help and Support

If additional support is required, Avnet has many avenues to search depending on your needs. For general question regarding Ultra96-V2, please visit our website at http://avnet.me/ultra96-v2. Here you can find documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding Ultra96-V2 hardware design, software application development, using Xilinx tools, training and other topics can be posted on the Ultra96-V2 Support Forum at http://avnet.me/Ultra96_forum. Avnet's technical support team monitors the forum during normal business hours in North America.

Those interested in customer-specific options on Ultra96-V2 can send inquiries to customize@avnet.com.