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UltraZed-EV™ Carrier Card Designer's Guide

Version 1.3

LIT# UltraZed-EV-SOM-Designer's-Guide-rev-1.3

Contents

1 Introduction

This document provides guidelines for designing custom Carrier Cards for the Avnet UltraZed-EV SOM. It includes reference schematics for implementing UltraZed-EV™ SOM external interfaces as well as the Carrier Card PCB design guidelines.

1.1 Glossary

Term	Definition
PS	Zynq UltraScale+ MPSoC Processing System
PL	Zynq UltraScale+ MPSoC Programmable Logic
MIO	PS Multiplexed Input Output Pins
POR	Power On Reset
APU	Application Processing Unit
RPU	Real-time Processing Unit
GPU	Graphics Processing Unit
SYSMON	System Monitor
HD	High Density PL I/O Pins
HP	High Performance PL I/O Pins
PMBus	Power Management Bus

1.2 Additional Documentation:

- Additional information and documentation on Xilinx's Zynq® UltraScale+™ MPSoC can be found at http://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html.

- Additional information and documentation on UltraZed-EV SOM or Carrier Card can be found at www.ultrazed.org/product/ultrazed-EV under the appropriate product page.

- Please Section 8, Getting Help and Support for further links.

2 UltraZed-EV SOM

UltraZed-EV™ SOM is a high performance, full-featured, System-On-Module (SOM) based on the Xilinx Zynq® UltraScale+™ MPSoC EV family of devices. Designed in a small form factor, the UltraZed-EV SOM packages all the necessary functions such as dual system memory, high-speed transceivers, Ethernet, USB, and configuration memory needed for an embedded video processing system. Although, initially released with the Xilinx XCZU7EV device, the UltraZed-EV SOM are pin and form factor compatible with the XCZU5EV/XCZU4EV or XCZU7EG/XCZU5EG/XCZU4EG (EG version of the UltraZed-EV SOM) versions using the MPSoC device in the same package as the XCZU7EV device.

The UltraZed-EV SOM is offered in extended and industrial temperatures and supports the following features:

- Xilinx XCZU7EV-1FBVB900 device
- PS DDR4 SDRAM (4GB, in x64 configuration)
- PL DDR4 SDRAM (1GB, in x16 configuration)
- 300 MHz LVDS system clock
- Dual QSPI Flash (64MB)
- I2C EEPROM (2Kb)
- eMMC Flash (8GB, x8)
- USB 2.0 ULPI PHY
- Gigabit Ethernet PHY
- I2C 8-bit I/O expander
- 2-channel I2C switch/mux
- PS reference clock input
- On-board voltage regulators
- Power-On Reset (POR) circuit
- Small 4-position boot mode DIP switch
- JX micro-header connectors (2 x 200-pin, 1 x 120-pin) providing the following connections to the Carrier Cards
    - 152 user PL I/O pins
    - 26 user PS MIO pins (one full MIO bank)
    - 4 PS GTR transceivers
    - 4 PS GTR reference clock inputs
    - 16 PL GTH transceivers
    - 8 PL GTH reference clock inputs
    - PS JTAG interface
    - PL SYSMON interface
    - USB 2.0 connector interface
    - Gigabit Ethernet RJ45 connector interface
    - PMBus interface
    - SOM PS VBATT battery input
    - Carrier Card I2C interface
    - SOM Reset input
    - Carrier Card interrupt input
    - Carrier Card Reset output
    - Power Good output

– SOM input voltages and output sense pins

The UltraZed-EV SOM high-level block diagram is shown in the following figure. The interfaces to the Zynq UltraScale+ MPSoC device on the UltraZed-EV SOM are divided into Processing System (PS) side and Programmable Logic (PL) side. The following sections describe the UltraZed-EV SOM on-board resources and external interfaces to the Carrier Cards.

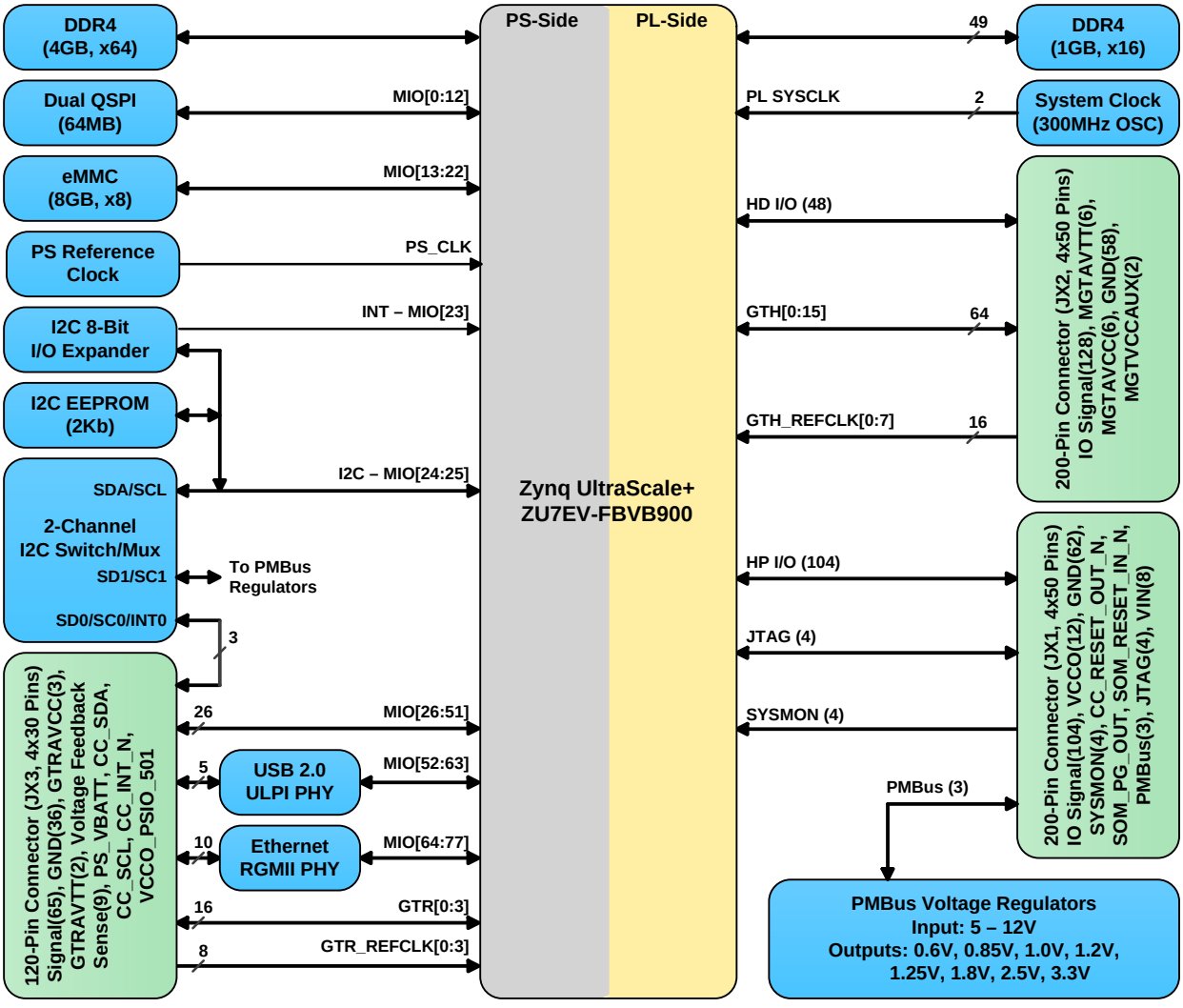


Figure 1 – UltraZed-EV SOM Block Diagram

3 UltraZed-EV SOM On-board Resources

The following sections provide a brief description of each component/resource available on the UltraZed-EV SOM. ***Please refer to the Avnet UltraZed-EV SOM schematic at the end of this document for more information on the UltraZed-EV SOM on-board resources***.

3.1 Zynq UltraScale+ MPSoC XCZU7EV-1FBVB900 Device

The UltraZed-EV SOM utilizes the Xilinx ***XCZU7EV-FBVB900*** device in -1 speed grade part (the UltraZed-EV SOM is designed to support all speed grades for the XCZU7EV-FBVB900 device). The ***XCZU7EV-1FBVB900*** device supports APU speed of 1.2GHz (max), RPU speed of 500MHz (max), GPU speed of 600MHz (max), and DDR4 speed of up to 2400Mbps. The ZU7EV-FBVB900 device features the following resources:

- 78 PS MIO pins (3 banks of MIOs, PS banks 500, 501, and 502, with 26 pins/bank)
- PS GTR transceivers along with 4 PS GTR reference clock inputs (PS bank 505)
- 16 PL GTH transceivers (PL quads 224 – 227)
- 8 PL GTH reference clock inputs (PL quads 224 – 227)
- PS DDR4 x64 interface (PS bank 504)
- PS JTAG interface (PS bank 503)
- Real-Time Clock (PS bank 503)
- PL SYSMON interface (PL bank 0)
- 48 PL HD (High Density) I/O pins (PL banks 47 and 48)
- 156 PL HP (High Performance) I/O pins (PL banks 64, 65, and 66)

The following sections provide brief descriptions of how each XCZU7EV MPSoC bank is used on the Avnet UltraZed-EV SOM followed by detail descriptions in subsequent sections.

3.1.1 PS MIO Bank 500

The PS MIO bank 500 consists of 26 MIO pins, MIO[0:25]. The MIO pins for this bank are operated at 1.8V and used to implement the following interfaces on the UltraZed-EV SOM:

- Dual Parallel (x8) QSPI Flash
- eMMC x8 Flash
- I2C EEPROM (2Kb)
- I2C 8-bit I/O expander
- I2C 2-channel switch/mux
- Carrier Card I2C interface
- I2C interface to the PMBus voltage regulators

3.1.2 PS MIO Bank 501

The PS bank 501 consists of 26 MIO pins, MIO[26:51]. These MIO pins are routed to the JX3 connector and are available to the custom Carrier Cards. The PS bank 501 I/O can be operated at 1.8V, 2.5V, or 3.3V set by the user via JX3 connector. This full bank of MIO pins can be used on a custom Carrier Card to implement various interfaces. On the Avnet UltraZed-EV Carrier Card, PS MIO bank 501 are operated at 3.3V and used to implement the following interfaces:

- microSD card
- Dual USB-UART ports

- PS PMOD header
- PS user LED
- PCIe Root Port reset
- DisplayPort auxiliary interface

3.1.3 PS MIO Bank 502

The PS bank 502 consists of 26 MIO pins, MIO[52:77]. The MIO pins for this bank are operated at 1.8V and used to implement the following interfaces on the UltraZed-EV SOM (please refer to the *USB 2.0 PHY* and *Ethernet PHY* sections of this document for more information):

- USB 2.0 ULPI PHY interface
- Gigabit Ethernet RGMII PHY interface

3.1.4 PS Bank 503

The PS bank 503 consists of JTAG, reset, PS reference clock input, boot mode, RTC crystal input, and few configuration pins. The reset, PS reference clock input, boot mode, RTC crystal input, and the configuration pins of the PS bank 503 pins are used on the UltraZed-EV SOM while the JTAG pins are routed to the JX1 connector. The PS bank 503 I/O is operated at 1.8V.

Zynq UltraScale+ MPSoC provides a built-in Real-Time Clock (RTC). A 32.768 KHz crystal is connected to the PS bank 503 ***PS_PADI*** and ***PS_PADO*** pins for the RTC. The on-chip RTC uses the ***PS_VBATT*** pin (provided by the Carrier Card via JX3 connector) for the backup battery. Carrier Cards drive the ***PS_VBATT*** pin with a 1.5V battery.

3.1.5 PS Bank 504

The PS bank 504 consists of DDR4 interface pins. These pins are used on the UltraZed-EV SOM to implement the DDR4 x64 memory interface. The PS bank 504 I/O is operated at 1.2V.

3.1.6 PS Bank 505

The PS bank 505 consists of PS GTR transceiver and their associated reference clock input pins (PS provides 4 GTR transceivers along with 4 reference clock inputs). These pins are routed to the JX3 connector and are available to the custom Carrier Cards. The GTR transceiver power rails (0.85V and 1.8V) are supplied by the custom Carrier Cards via JX3 connector.

3.1.7 PL Bank 47, 48, 64, 65, and 66

The PL HD banks 47 and 48 and HP banks 64, 65, and 66 provide 48 HD (High Density, banks 47 and 48) and 156 HP (High Performance, banks 64, 65, and 66) I/O pins. The following shows how the PL HD and HP pins are used on the UltraZed-EV SOM.

- HP bank 66 is used to implement a PL x16 DDR4 interface on the UltraZed-EV SOM.
- HP banks 64 and 65 I/O pins are routed to the JX1 connector and are available to the custom Carrier Cards (each bank provides 24 differential pairs and 4 single-ended I/O).
- The 48 HD I/O pins are routed to the JX2 connector and are available to the custom Carrier Cards. These pins can be used as 24 differential input pairs or 48 single-ended I/O.

The PL HP banks I/O pins can be operated at 1.0V – 1.8V while the PL HD bank I/O pins can be operated at 1.2V – 3.3V. The VCCO voltages for the PL HD and HP banks are provided by the custom Carrier Cards via JX1 connector.

3.1.8 PL Bank 0

The PL bank 0 consists of System Monitor (***SYSMON***) pins. These pins are routed to the JX1 connector and are available to the custom Carrier Cards. The System Monitor supply voltages (VCCADC and VREF) are provided on the UltraZed-EV SOM.

3.1.9 PL Quad 224, 225, 226, and 227 GTH Transceivers

The ZU7EV PL provides 16 GTH transceivers in 4 quads (224, 225, 226, and 227). Each GTH quad has 2 differential reference clock inputs. The following figure shows how the PL GTH transceivers are used on the UltraZed-EV SOM. All 16 GTH transceivers along with 8 differential reference clock inputs are routed to the Carrier Card via JX2 connector.

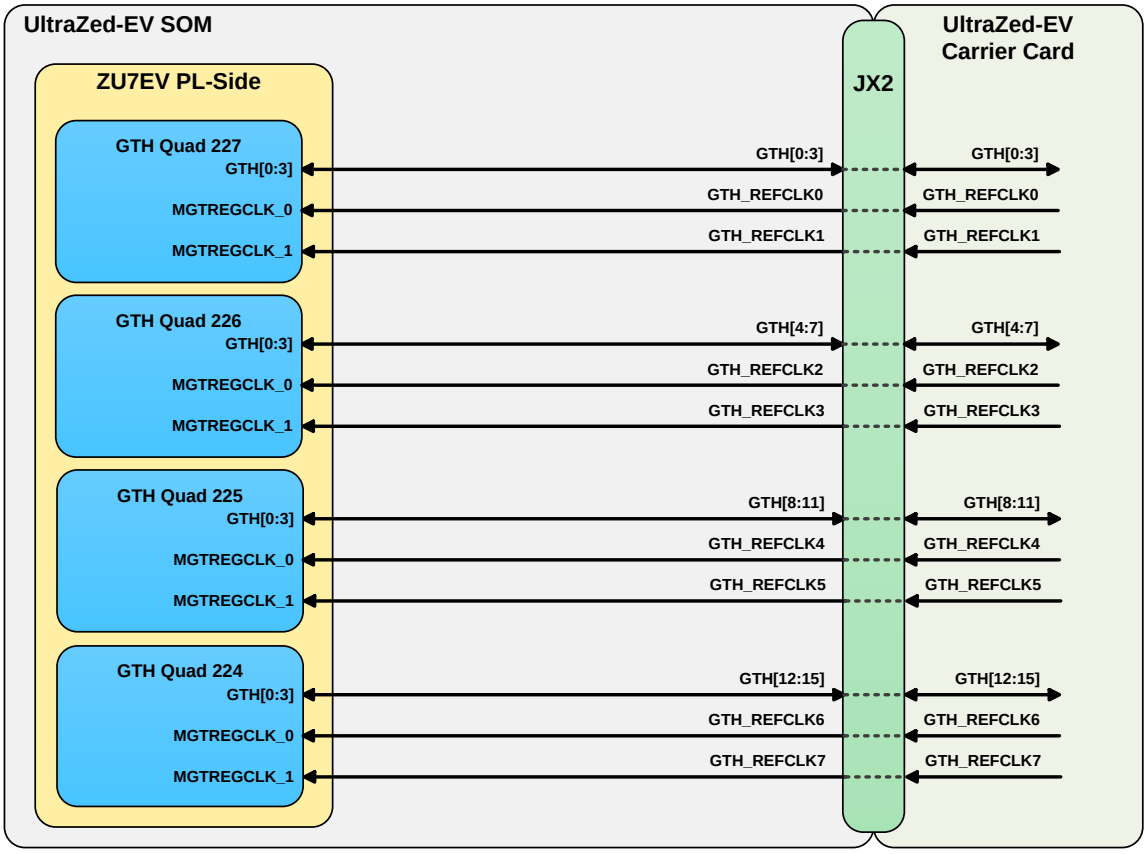


Figure 2 – PL GTH Transceiver Usage on the UltraZed-EV SOM

3.2 PS Reference Clock Input

The UltraZed-EV SOM provides a 33.33 MHz single-ended 1.8V reference clock input to the Zynq UltraScale+ MPSoC PS block.

3.3 I2C EEPROM

The UltraZed-EV SOM provides 2Kb of I2C EEPROM using the Atmel ***AT34C02D-MAHM-T*** (8-pin UDFN package) device. The EEPROM device are connected to the PS I2C bus (PS bank 500 MIO[24:25]) and operated at VCC of 1.8V. This EEPROM can be used to store system level parameters/data.

3.4 Dual Parallel QSPI Flash

The UltraZed-EV SOM provides 64MB of QSPI Flash in dual-parallel (x8) configuration. Two Micron ***MT25QU256ABA1EW7-0SIT*** (8-pin W-PDFN package) devices are used to implement the parallel Flash interface on the UltraZed-EV SOM. The QSPI Flash devices are connected to the PS MIO bank 500 and operated at 1.8V I/O. The QSPI Flash can be used as a primary boot device on the UltraZed-EV SOM.

Table 1 – Dual-Parallel QSPI Flash Interface Pin Assignments

Signal Name	MIO Pin #	Notes
CLK_1	MIO[0]	Lower QSPI device clock
DATA[1]_1	MIO[1]	Lower QSPI device DATA[1]
DATA[2]_1	MIO[2]	Lower QSPI device DATA[2]
DATA[3]_1	MIO[3]	Lower QSPI device DATA[3]
DATA[0]_1	MIO[4]	Lower QSPI device DATA[0]
CS_1	MIO[5]	Lower QSPI device chip select
Feedback CLK	MIO[6]	No Connect
CS_2	MIO[7]	Upper QSPI device chip select
DATA[0]_2	MIO[8]	Upper QSPI device DATA[0]
DATA[1]_2	MIO[9]	Upper QSPI device DATA[1]
DATA[2]_2	MIO[10]	Upper QSPI device DATA[2]
DATA[2]_2	MIO[11]	Upper QSPI device DATA[3]
CLK_2	MIO[12]	Upper QSPI device clock

3.5 eMMC Flash

The UltraZed-EV SOM provides 8GB of eMMC Flash to be used as a primary and/or secondary boot device. A single Micron ***MTFC8GAKAJCN-4M IT*** (153-pin VFBGA package) device is used to implement the eMMC Flash x8 interface. The eMMC device is connected to the PS MIO bank 500 and operated at 1.8V I/O. P0 port of the SOM I2C 8-bit I/O expander can be used to soft reset the eMMC device (please refer to the *I2C 8-Bit I/O Expander* section of this document for more information). The following table shows the eMMC Flash connections to the Zynq MPSoC device.

Table 2 – eMMC Flash Interface Pin Assignments

Signal Name	MIO Pin #	Notes
DATA[0]	MIO[13]	eMMC DATA[0]
DATA[1]	MIO[14]	eMMC DATA[1]
DATA[2]	MIO[15]	eMMC DATA[2]
DATA[3]	MIO[16]	eMMC DATA[3]
DATA[4]	MIO[17]	eMMC DATA[4]
DATA[5]	MIO[18]	eMMC DATA[5]

DATA[6]	MIO[19]	eMMC DATA[6]
DATA[7]	MIO[20]	eMMC DATA[7]
CMD	MIO[21]	eMMC Command
CLK	MIO[22]	eMMC Clock

3.6 MPSoC Real-Time Clock (RTC)

Zynq UltraScale+ MPSoC provides a built-in Real-Time Clock (RTC). A 32.768 KHz crystal is connected to the PS bank 503 ***PS_PADI*** and ***PS_PADO*** pins for the RTC. The on-chip RTC uses the ***PS_VBATT*** pin (provided by the custom Carrier Card via JX3 connector) for the backup battery. Custom Carrier Cards drive the ***PS_VBATT*** pin with a 1.5V battery.

3.7 PS DDR4 SDRAM

The UltraZed-EV SOM provides 4GB of PS DDR4 memory in x64 configuration using 4 Micron ***MT40A512M16JY-083E IT:B*** (96-pin BGA package) x16 devices . This device is implemented in 512Mb x 16 configuration and supports up to 2400Mbps data rate. The DDR4 devices are connected to the PS bank 504 and operated at 1.2V.

3.8 USB 2.0 PHY

The UltraZed-EV SOM provides a single USB 2.0 PHY interface using the Microchip ***USB3320*** USB 2.0 ULPI PHY in 32-pin QFN package. The USB 2.0 ULPI PHY connector side (connected to the JX3 connector) along with the PS USB 3.0 port (PS GTR[x]), connected to the JX3 connector) can be used on custom Carrier Cards to implement a USB 2.0/3.0 interface via a single connector. Please refer to the *UltraZed-EV SOM External Interfaces* section of this document for more information.

The USB 2.0 ULPI PHY host side I/O is connected to the PS MIO bank 502 and operated at 1.8V on the UltraZed-EV SOM. P1 port of the I2C 8-bit I/O expander can be used to soft reset the USB 2.0 ULPI PHY (please refer to the *I2C 8-Bit I/O Expander* section of this document for more information).

Table 3 – USB 2.0 ULPI PHY Host Interface Side Pin Assignments

Signal Name	MIO Pin #	Notes
CLK	MIO[52]	ULPI PHY clock input
DIR	MIO[53]	Controls the direction of the data bus
DATA[2]	MIO[54]	Host side DATA[2]
NXT	MIO[55]	This signal is used to throttle the data
DATA[0]	MIO[56]	Host side DATA[0]
DATA[1]	MIO[57]	Host side DATA[1]
STP	MIO[58]	Stops the data stream currently on the bus
DATA[3]	MIO[59]	Host side DATA[3]
DATA[4]	MIO[60]	Host side DATA[4]
DATA[5]	MIO[61]	Host side DATA[5]
DATA[6]	MIO[62]	Host side DATA[6]

DATA[7]	MIO[63]	Host side DATA[7]

3.9 Ethernet PHY

The UltraZed-EV SOM provides a single Gigabit Ethernet PHY interface using the Marvell ***88E1512*** RGMII PHY device in 56-pin QFN package. The UltraZed-EV SOM Gigabit Ethernet PHY connector side (connected to the JX3 connector) along with an RJ45 connector located on the custom Carrier Card can be used to implement a Gigabit Ethernet port.

The Marvell 88E1512 RGMII Ethernet PHY host side I/O is connected to the PS MIO bank 502 and operated at 1.8V on the UltraZed-EV SOM. P2 port of the I2C 8-bit I/O expander can be used to soft reset the Gigabit Ethernet PHY. P3 port of this I/O expander is connected to the Gigabit Ethernet PHY ***INT*** output. (Please refer to the *I2C 8-Bit I/O Expander* section of this document for more information).

Table 4 – RGMII PHY Interface Host Interface Side Pin Assignments

Signal Name	MIO Pin #	Notes
TX_CLK	MIO[64]	Transmit clock
TX_DATA[0]	MIO[65]	Transmit DATA[0]
TX_DATA[1]	MIO[66]	Transmit DATA[1]
TX_DATA[2]	MIO[67]	Transmit DATA[2]
TX_DATA[3]	MIO[68]	Transmit DATA[3]
TX_CTL	MIO[69]	Transmit control
RX_CLK	MIO[70]	Receive clock
RX_DATA[0]	MIO[71]	Receive DATA[0]
RX_DATA[1]	MIO[72]	Receive DATA[1]
RX_DATA[2]	MIO[73]	Receive DATA[2]
RX_DATA[3]	MIO[74]	Receive DATA[3]
RX_CTL	MIO[75]	Receive control
MDC	MIO[76]	Management Data Clock
MDIO	MIO[77]	Management Data I/O

3.10 PL System Clock Input

The UltraZed-EV SOM provides a 300 MHz LVDS system clock input to the PL bank 66 to be used primarily for the PL DDR4 interface. The following figure shows the system clock connection to the bank 66.

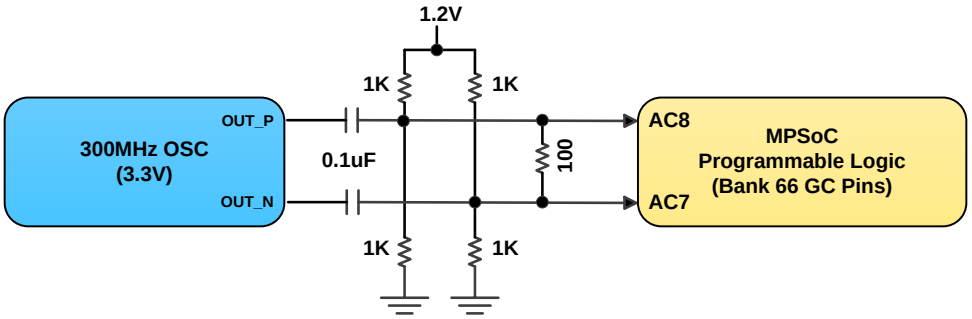


Figure 3 – 300MHz PL System Clock

3.11 I2C 8-Bit I/O Expander

The UltraZed-EV SOM uses the ON Semi ***PCA9654E*** I2C 8-bit I/O expander device in the 16-pin TSSOP package for generating various resets and control signals on the UltraZed-EV SOM. The I2C 8-bit I/O expander device is connected to the PS I2C bus (PS bank 500 MIO[24:25]) and operated at VCC of 1.8V. The interrupt output (***INT#***) of the PCA9654E device is connected to the PS MIO[23]. The following table shows how the I/O expander ports are used.

Note: ***On power-up all I/O expander ports default to inputs. With the on-board pull-ups on all ports, all output reset signals shown in the following table are in their inactive state***.

Table 5 – I2C I/O Expander Port Usage

IO Expander Port	Direction	Usage
P0	Output	eMMC soft reset
P1	Output	USB 2.0 ULPI PHY soft reset
P2	Output	Gigabit Ethernet PHY soft reset
P3	Input	Gigabit Ethernet PHY interrupt
P4	Input	2-channel I2C switch/mux interrupt input
P5	Input	This port is connected to the *PMBus_ALERT_N* signal of the UltraZed-EV SOM PMBus regulators and used along with the channel 1 of the I2C 2-channel switch/mux (connected to the PMBus regulator I2C signals) to perform power management on the UltraZed-EV SOM and the Carrier Card. Please refer to the *PMBus Interface* section of this document for more information.
P6	Output	2-channel I2C switch/mux soft reset
P7	Output	Active low Carrier Card Reset output (*P7_CC_RST_N*). Please refer to the *Carrier Card Reset Output* section of this document for more information.

3.12 2-Channel I2C Switch/Mux

The UltraZed-EV SOM uses a 2-channel I2C switch/mux to expand the PS I2C bus (PS bank 500 MIO[24:25]). The NXP ***PCA9543APW*** device in the 14-pin TSSOP package is used for this interface. The use of this I2C switch/mux provides a nice isolation so that devices connected to the I2C bus on the UltraZed-EV SOM and the I2C slave devices on the custom Carrier Cards as well

as the voltage regulators connected the PMBus I2C are not physically placed on the same I2C bus as shown in Figure 1.

The PCA9543APW may also be used for voltage translation, allowing the use of different bus voltages on each SD/SC pair such that 1.8V, 2.5V, or 3.3V devices can communicate with the PS 1.8V I2C MIO pins. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel. The PCA9543A VCC must be connected to the 2.5V rail (please refer to the PCA9543A datasheet for more information).

P6 port of the I2C 8-bit I/O expander can be used to soft reset the 2-channel I2C switch/mux device. The following table shows how each PCA9543A channel are used.

Table 6 – I2C Switch/Mux Channel Usage

I2C Switch Channel	Usage	Notes
Master Channel (SDA/SCL/INT)	This channel is connected to the PS I2C port, MIO[24:25] and operated at 1.8V. The master *INT* output is connected to the P4 port of the I2C 8-bit I/O expander.	Pulled-up to 1.8V On the SOM
Slave Channel 0 (SD0/SC0/INT0)	This channel is connected to the JX3 connector (*CC_SDA*, *CC_SCL*, and *CC_INT_N* signals) to allow slave I2C devices on the Carrier Card to be virtually placed on the same PS I2C bus (MIO[24:25]) as the I2C devices on the UltraZed-EV SOM so that software can use a single PS I2C core to communicate will all I2C devices in the system. Please refer to the *Carrier Card I2C Interface* section of this document for more information.	Pulled-up to 1.8V, 2.5V, or 3.3V On the Carrier Card
Slave Channel 1 (SD1/SC1/INT1)	This channel is connected to the PMBus (*PMBus_DATA* and *PMBus_CLK* signals) of the UltraZed-EV SOM PMBus voltage regulators and used to control all PMBus voltage regulators on the UltraZed-EV SOM as well as the Carrier Card (the PMBus is connected to the Carrier Card via JX1 connector). This feature allows the PS to control/monitor the PMBus voltage regulators on the UltraZed-EV SOM as well as the Carrier Card for the purpose of power management and/or measurements. Please refer to the *PMBus Interface* section of this document for more information.	Pulled-up to 3.3V On the SOM The unused slave channel 1 *INT1* input is pulled up to the VCC (2.5V) rail.

3.13 PL DDR4 SDRAM

The UltraZed-EV SOM provides 1GB of PL DDR4 memory (needed for video applications) in x16 configuration using Micron ***MT40A512M16JY-083E IT:B*** device (96-pin BGA package). This device is implemented in 512Mb x 16 configuration and supports up to 2400Mbps data rate. This

DDR4 device is connected to the PL HP bank 66 and operated at 1.2V. The following table shows the PL DDR4 interface pinout.

Table 7 – Pinout for PL DDR4 Interface

DDR4 Signal	MPSoC PL Bank	MPSoC PL Pin #
DDR4_A0	66	AC9
DDR4_A1	66	AD9
DDR4_A2	66	AC6
DDR4_A3	66	AD6
DDR4_A4	66	W8
DDR4_A5	66	Y8
DDR4_A6	66	AA8
DDR4_A7	66	AB8
DDR4_A8	66	W9
DDR4_A9	66	AC12
DDR4_A10	66	AD12
DDR4_A11	66	AA12
DDR4_A12	66	AA11
DDR4_A13	66	AB11
DDR4_BA0	66	AB9
DDR4_BA1	66	AB10
DDR4_BG	66	Y10
DDR4_CAS_N	66	AD11
DDR4_RAS_N	66	AD10
DDR4_WE_N	66	AC11
DDR4_CKE	66	AE7
DDR4_CS_N	66	AA10
DDR4_ODT	66	AE3
DDR4_RESETN	66	Y1
DDR4_ACTN	66	AE2
DDR4_CK_T	66	Y7
DDR4_CK_C	66	AA7
DDR4_DM_DBI_N[1]	66	AD7
DDR4_DM_DBI_N[0]	66	AD2
DDR4_DQS1_T	66	AD4
DDR4_DQS1_C	66	AE4
DDR4_DQS0_T	66	AA3
DDR4_DQS0_C	66	AB3
DDR4_DQ15	66	AA5

DDR4_DQ14	**66**	**AA6**
DDR4_DQ13	**66**	**AC4**
DDR4_DQ12	**66**	**AB4**
DDR4_DQ11	**66**	**AE5**
DDR4_DQ10	**66**	**AD5**
DDR4_DQ9	**66**	**AB5**
DDR4_DQ8	**66**	**AB6**
DDR4_DQ7	**66**	**AA1**
DDR4_DQ6	**66**	**AA2**
DDR4_DQ5	**66**	**AC1**
DDR4_DQ4	**66**	**AB1**
DDR4_DQ3	**66**	**AC2**
DDR4_DQ2	**66**	**AC3**
DDR4_DQ1	**66**	**AE1**
DDR4_DQ0	**66**	**AD1**
SYSCLK_P (300 MHz LVDS Clock Source)	**66**	**AC8**
SYSCLK_N (300 MHz LVDS Clock Source)	**66**	**AC7**
VRP DCI resistor (bank 66, 240 Ohms pull-down)	**66**	**Y9**
VREF (bank 66) – 1K pull-up/pull-down divider on the 1.2V rail	**66**	**W10**
PL SYS_RST – Can be driven by the Carrier Card	**64 or 65**	

3.14 PMBus Interface

PMBus is used on the UltraZed-EV SOM to program/control/monitor all on-board PMBus voltage regulators. The UltraZed-EV SOM has access to the Carrier Card PMBus header via the JX1 connector (***PMBus_DATA***, ***PMBus_CLK***, and ***PMBus_ALERT_N*** signals). The Carrier Card PMBus header along with a programming dongle can be used to program all UltraZed-EV SOM PMBus voltage regulators.

An UltraZed-EV custom Carrier Card can provide a PMBus header for programming of all PMBus voltage regulators on the Carrier Card as well as the PMBus voltage regulators on the UltraZed-EV SOM, but it is not required to do so. The PMBus regulators on the UltraZed-EV SOM are pre-programmed prior to shipment. However, if programming of PMBus voltage regulators on a custom Carrier Card is required, the custom Carrier Card must implement the PMBus header.

After the initial programming of all PMBus voltage regulators, the UltraZed-EV SOM can drive the PMBus (via channel 1 of the I2C switch/mux and P5 port of the I2C 8-bit I/O expander) in order to control/monitor the PMBus voltage regulators on the UltraZed-EV SOM for the purpose of power management and/or measurements. If the PMBus is implemented on the custom Carrier Card, the UltraZed-EV SOM PMBus can monitor/control the Carrier Card PMBus voltage regulators as well. ***If not used, the UltraZed-EV SOM PMBus interface must be left unconnected on custom Carrier Cards so that the UltraZed-EV SOM can still control/monitor its on-board PMBus regulators***. The following figure shows how the PMBus is connected on the UltraZed-EV SOM and the Avnet Carrier Card.

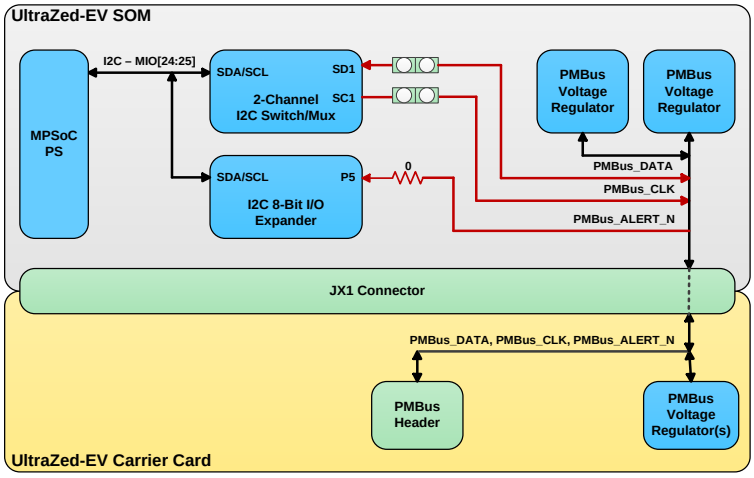


Figure 4 – UltraZed-EV SOM PMBus Interface

3.15 SOM Reset Structure

The following figure shows the reset structure for the MPSoC device and the Carrier Card. The reset operation for the peripherals connected to the MPSoC on the UltraZed-EV SOM are as follows:

- ***eMMC Device*** – This device can only be reset via the ***P0*** port of the I2C 8-bit I/O expander.
- ***USB 2.0 ULPI PHY*** – This device can be reset via ***PS_POR_B***, ***PS_SRST_B***, or the ***P1*** port of the I2C 8-bit I/O expander.
- ***Gigabit Ethernet PHY*** – This device can be reset via ***PS_POR_B***, ***PS_SRST_B***, or the ***P2*** port of the I2C 8-bit I/O expander.
- ***2-Channel I2C Switch/Mux Device*** – This device can be reset via ***PS_POR_B***, ***PS_SRST_B***, or the ***P6*** port of the I2C 8-bit I/O expander.

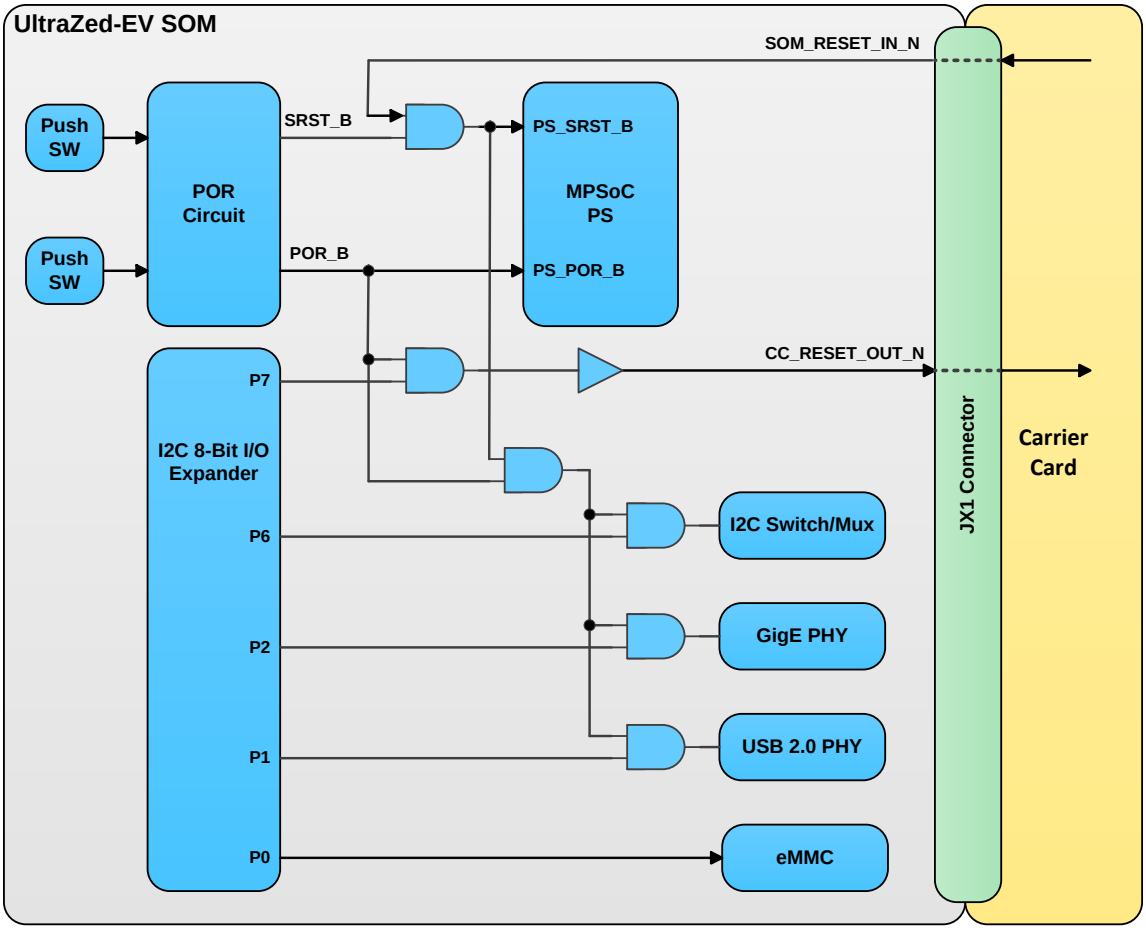


Figure 5 – UltraZed-EV SOM Reset Structure

3.16 PS Power-On Reset (POR) Circuit

The Power-On Reset (POR) circuit for the MPSoC device is implemented on the UltraZed-EV SOM. This circuit generates the ***PS_POR_B*** as well as the ***PS_SRST_B*** signals. Two small push switches (SW3 and SW4) can be used to manually assert the ***PS_POR_B*** as well as the ***PS_SRST_B*** signals as shown in the following figure. **The *PS_POR_B* and the *PS_SRST_B* push switches are not populated on the production SOMs shipped to customers**.

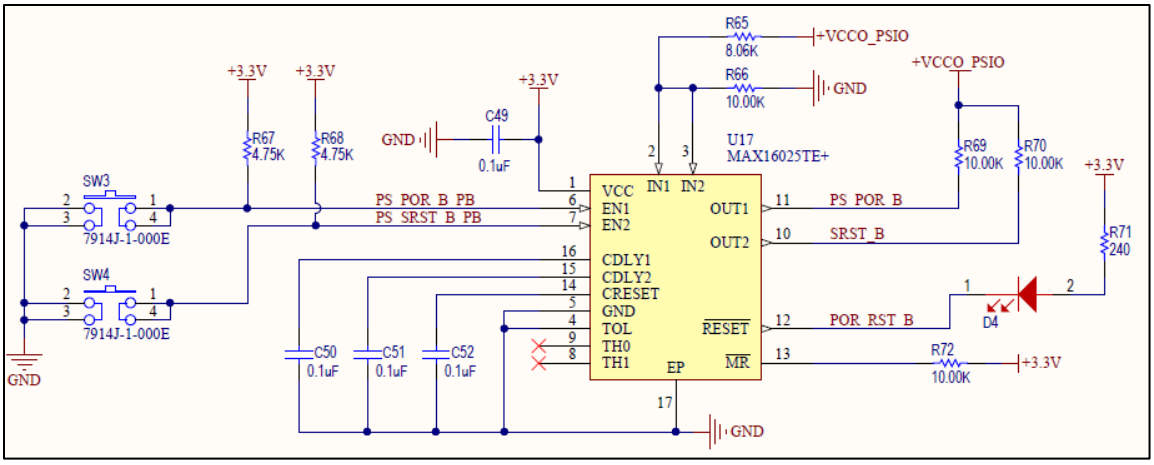


Figure 6 – PS Power-up Reset Circuit

3.17 SOM Reset Input

The UltraZed-EV SOM can be reset via an ***active low*** reset signal from the custom Carrier Card (***SOM_RESET_IN_N***) connected to the JX1 connector. The ***SOM_RESET_IN_N*** signal can be used to reset the MPSoC device as well as all other device on the UltraZed-EV SOM. The ***SOM_RESET_IN_N*** signal must be a 1.8V input signal and it is pulled up on the UltraZed-EV SOM. If not used, the ***SOM_RESET_IN_N*** signal must be left unconnected on the custom Carrier Cards. The ***SOM_RESET_IN_N*** signal must have a minimum pulse width of ***3xPS_CLK or 90ns***, required by the UltraZed-EV SOM.

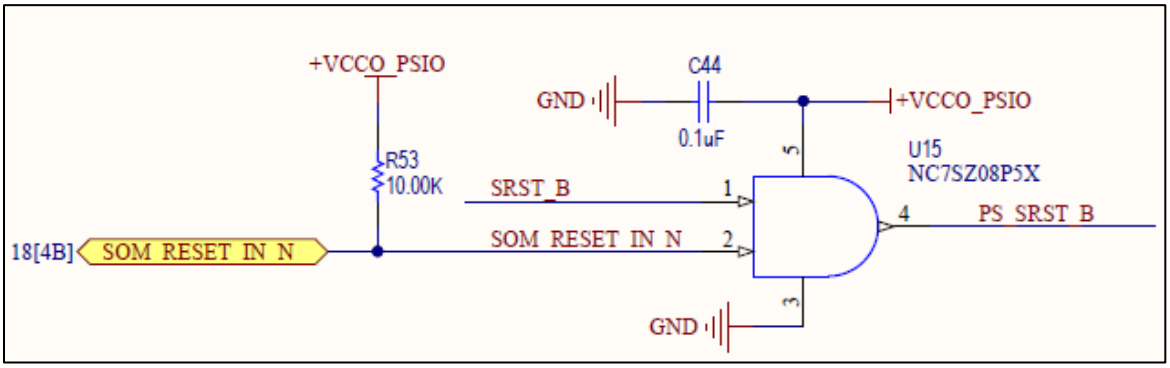


Figure 7 – SOM Input Reset Circuit

3.18 Carrier Card Reset Output

The UltraZed-EV SOM provides an ***active low*** reset signal to the Carrier Card (***CC_RESET_OUT_N***) via JX1 connector. The ***CC_RESET_OUT_N*** signal can be used to reset any device on the Carrier Card. The ***CC_RESET_OUT_N*** signal are generated by ANDing the PS Power-On Reset (***PS_POR_B*** signal) and the P7 port of the I2C 8-bit I/O expander device (***P7_CC_RST_N*** signal) together as shown in the following figure (the below circuit uses a NAND

gate along with an inverter to make the ***CC_RESET_OUT_N*** signal 1.8V/2.5V/3.3V capable). The ***CC_RESET_OUT_N*** signal must be pulled up to 1.8V, 2.5V, or 3.3V on the Carrier Card.

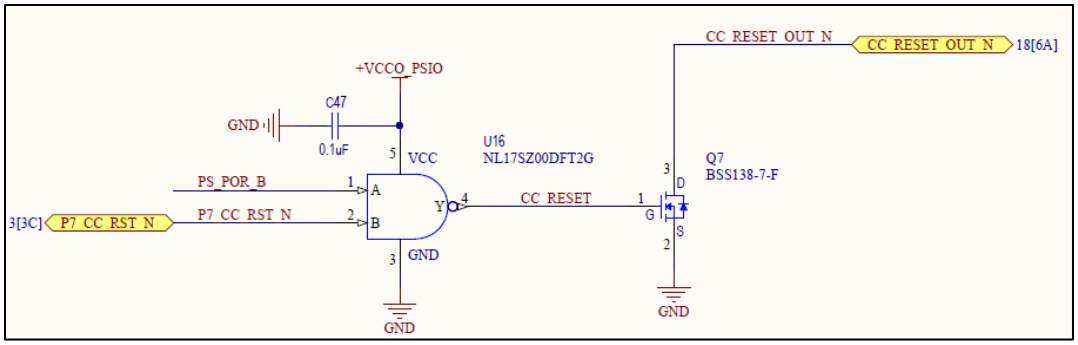
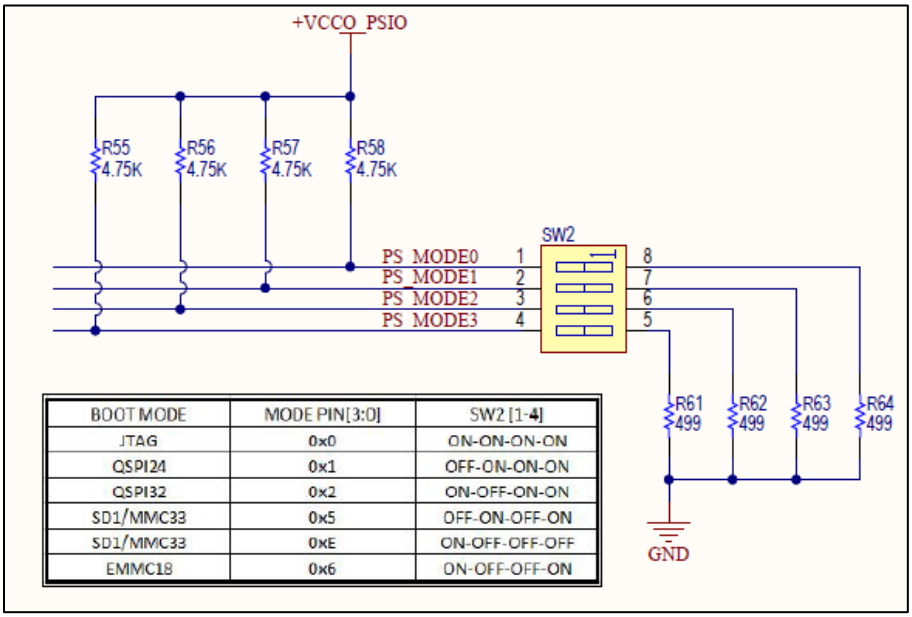


Figure 8 – Carrier Card Output Reset Circuit

3.19 PS Boot Mode Switch

The UltraZed-EV SOM uses a small 4-position DIP switch for the PS Boot Mode pins. This switch is connected to the MODE[3:0] pins of the PS bank 503 and allows users to select the PS primary boot device.



BOOT MODE	MODE PIN[3:0]	SW2 [1-4]
JTAG	0x0	ON-ON-ON-ON
QSPI24	0x1	OFF-ON-ON-ON
QSPI32	0x2	ON-OFF-ON-ON
SD1/MMC33	0x5	OFF-ON-OFF-ON
SD1/MMC33	0xE	ON-OFF-OFF-OFF
EMMC18	0x6	ON-OFF-OFF-ON

Figure 9 – PS Boot Mode Switch

3.20 MPSoC Heat Sink with Fan

The UltraZed-EV SOM uses a heat sink with fan for the MPSoC device. Users can use either a 5V or a 12V fan with the UltraZed-EV SOM heat sink (The UltraZed-EV SOM is shipped with a 5V fan). The fan header is located on the UltraZed-EV Carrier Card. Please refer to the *Carrier Card PCB Design Guideline* section of this document for more information.

NOTE: The heatsink with fan provided with the UltraZed-EV SOM is designed to be appropriate for most use cases except for the industrial high temperature extremes. It is expected that a system

designer will perform worst case analysis of the thermal environment of the final solution and devise a proper thermal solution for the challenges presented in the operating environment.

3.21 Voltage Regulators

Voltage regulators are used on the UltraZed-EV SOM to provide power to all components/interfaces used on the UltraZed-EV SOM. Power for the components/interfaces implemented on the Carrier Card are supplied by the Carrier Card (these will consist of, but not limited to all the interfaces/components that will utilize the UltraZed-EV SOM PS GTR transceivers, PS MIO bank 501, PL GTH transceivers, and/or PL HD/HP banks).

The UltraZed-EV SOM receives an input voltage of 5 – 12V from the custom Carrier Card and generates the voltage rails needed on the UltraZed-EV SOM using two PMBus voltage regulators. The UltraZed-EV SOM power architecture supports all speed grades offered for the ZU7EV-B900 device.

The UltraZed-EV SOM requires the following voltage rails to be supplied by the custom Carrier Cards. Please refer to the *Power Requirements* and the *UltraZed-EV SOM External Interfaces* sections of this document for more information.

- 5 – 12V main input voltage via JX1 connector
- PS MGTRAVCC (0.85V) via JX3 connector
- PS MGTRAVTT (1.8V) via JX3 connector
- PL MGTAVCC (0.9V) via JX2 connector
- PL MGTAVTT(1.2V) via JX2 connector
- PL MGTVCCAUX (1.8V) via JX2 connector
- PS MIO bank 501 VCCO (1.8V, 2.5V, or 3.3V) via JX3 connector
- PL HP bank 64 VCCO (1.0V – 1.8V) via JX1 connector
- PL HP bank 65 VCCO (1.0V – 1.8V) via JX1 connector
- PL HD bank 47 VCCO (1.2V – 3.3V) via JX1 connector
- PL HD bank 48 VCCO (1.2V – 3.3V) via JX1 connector
- PS VBATT (1.5V) via JX3 connector

4 UltraZed-EV SOM External Interfaces

The UltraZed-EV SOM provides sufficient resources to the custom Carrier Cards to implement fully customized systems that meet their application requirements. The UltraZed-EV SOM provides the following external interfaces to the custom Carrier Cards (signal directions are with respect to the UltraZed-EV SOM):

- 26 PS MIO pins (PS MIO bank 501, MIO[26:51])
- PS GTR transceivers
- 4 PS GTR reference clock inputs
- 16 PL GTH transceivers

- 8 PL GTH reference clock inputs
- PS JTAG interface
- PL SYSMON interface
- PMBus interface
- Carrier Card I2C interface
- SOM PS VBATT input
- SOM Reset input
- SOM input power
- Carrier Card interrupt input
- Carrier Card Reset output
- SOM Power Good output
- USB 2.0 connector interface
- Gigabit Ethernet RJ45 connector interface
- 48 PL HD (High Density) I/O pins (2 banks)
- 104 PL HP (High Performance) I/O pins (2 banks)

The 4 PS GTR transceivers along with the 4 GTR reference clock inputs available via UltraZed-EV SOM JX3 connector can be used to implement the following interfaces on the custom Carrier Cards:

- USB 3.0 interface
- PCIe Endpoint or Root Port interface
- SATA Host interface
- Display Port interface.

The 26 PS Multiplexed I/O (MIO) pins available via UltraZed-EV SOM JX3 connector can be used to implement a variety of interfaces on the custom Carrier Cards including, but not limited to:

- SD card interface
- CAN, UART, I2C, SPI interfaces
- General-purpose I/O (GPIO)

The PL HD and HP general-purpose I/O pins as well as the PL GTH transceiver pins can be used to implement a variety of interfaces on the custom Carrier Cards. Please refer to the Avnet ***UltraZed-EV Carrier Card Users Guide*** on the www.ultrazed.org/product/ultrazed-ev-carrier-card website for examples of interfaces implemented using the PL HD and HP I/O pins.

The following figure shows the UltraZed-EV SOM external interfaces followed by a brief description of each interface and how to design for it on the custom Carrier Cards.

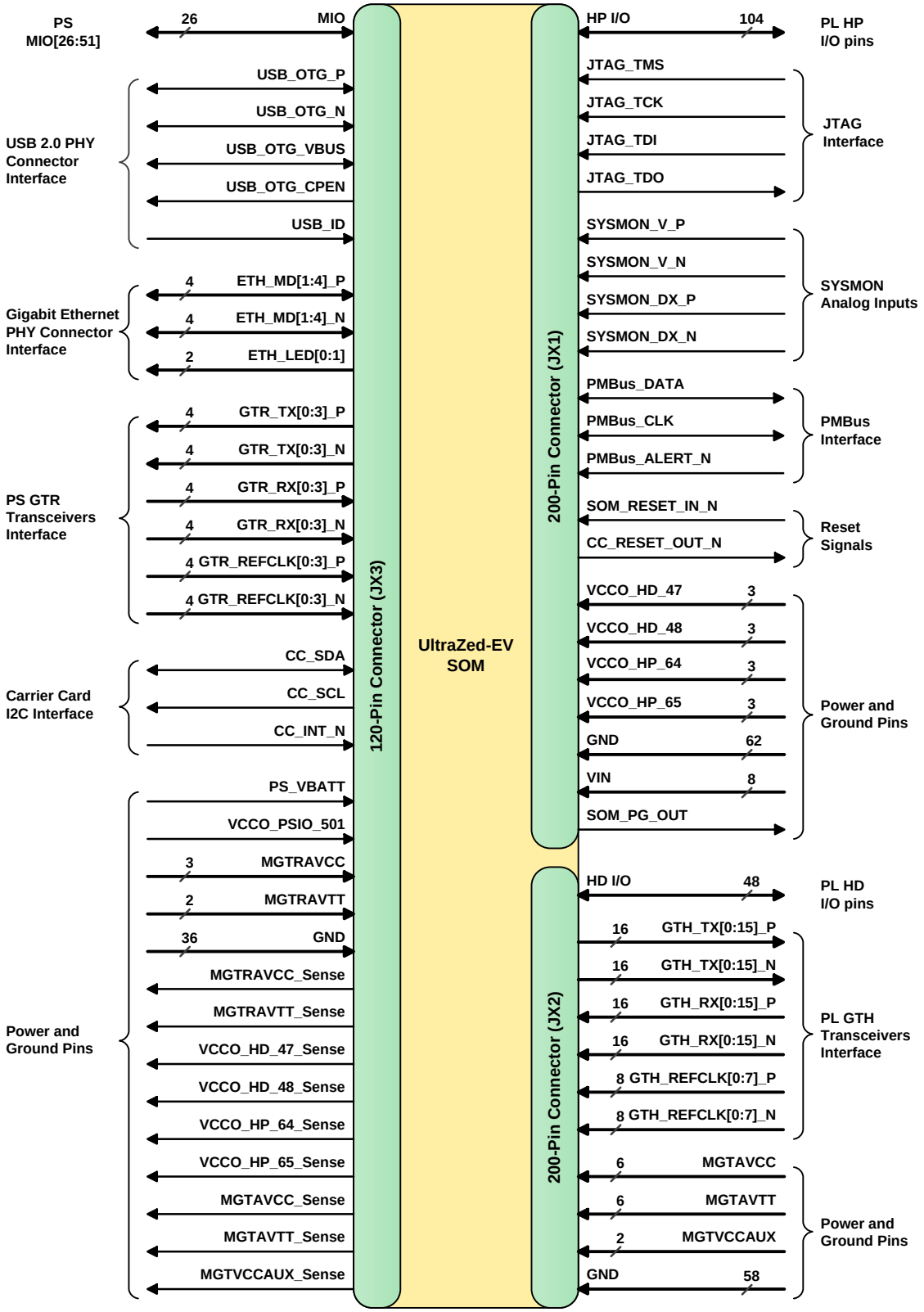


Figure 10 – UltraZed-EV SOM External Interfaces

Table 8 – UltraZed-EV SOM External Interface Signals

Signal Name	# of Pins	Description
MIO[26:51]	26	PS MIO Interface – 26 MIO pins from PS bank 501.
USB_OTG_P, USB_OTG_N, USB_ID, USB_OTG_VBUS, USB_OTG_CPEN	5	USB 2.0 PHY Interface – These pins are used by the custom Carrier Cards to implement a USB 2.0 interface. Please refer to the USB3320 datasheet for AC and DC spec of these signals.
ETH_MD[1:4]_P, ETHMD[1:4]_N, ETH_PHY_LED[0:1]	10	Gigabit Ethernet PHY Interface – These pins are used by the custom Carrier Cards to implement a Gigabit Ethernet interface. Please refer to the DP83867 datasheet for AC and DC spec of these signals.
GTR_TX[0:3]_P, GTR_TX[0:3]_N, GTR_RX[0:3]_P, GTR_RX[0:3]_N, GTR_REFCLK[0:3]_P, GTR_REFCLK[0:3]_N	24	PS GTR Transceivers Interface – These PS transceiver data and clock signals are used by the custom Carrier Cards to implement PCIe, SATA, DisplayPort, and USB 3.0 interfaces. Please refer to the Xilinx DS925 (Zynq UltraScale+ MPSoC datasheet) datasheet for AC and DC spec of these signals.
GTH_TX[0:15]_P, GTH_TX[0:15]_N, GTH_RX[0:15]_P, GTH_RX[0:15]_N, GTH_REFCLK[0:7]_P, GTH_REFCLK[0:7]_N	80	PL GTH Transceivers Interface – These PL transceiver data and clock signals are used by the custom Carrier Cards to implement various interfaces. Please refer to the Xilinx DS925 (Zynq UltraScale+ MPSoC datasheet) datasheet for AC and DC spec of these signals.
CC_SDA, CC_SCL, CC_INT_N	3	Carrier Card I2C Interface – This I2C interface are used to interface to the custom Carrier Cards I2C slave devices.
HP I/O	104	PL HP I/O – These pins are connected to the PL banks 64, and 65. These signals can be used by the custom Carrier Cards as single-ended or differential I/O. Please refer to the Xilinx UG571 and DS925 for more information on the PL High Performance (HP) I/Os.
HD I/O	48	PL HD I/O – These pins are connected to the PL banks 47 and 48. These signals can be used by the custom Carrier Cards as single-ended or differential input. Please refer to the Xilinx UG571 and DS925 for more information on the PL High Density (HD) I/Os.
JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO	4	JTAG Interface – These pins are used to interface to the MPSoC JTAG port and driven by a JTAG cable on the custom Carrier Cards.
SYSMON_V_P, SYSMON_V_N, SYSMON_DX_P, SYSMON_DX_N	4	SYSMO Interface – Custom Carrier Cards can use these pins to drive low speed analog signals into the PL System Monitor interface. Please refer to the Xilinx UG580 and DS925 for more information on the System Monitor interface.
PMBus_DATA, PMBus_CLK, PMBus_ALERT_N	3	PMBus Interface – This PMBus I2C interface is used to program and/or monitor the PMBus voltage regulators on the SOM as well as custom Carrier Cards (optional).

SOM_RESET_IN_N, CC_RESET_OUT_N	2	Reset Signals – These reset signals are used to reset the SOM or the devices on the custom Carrier Cards.
VCCO_HP_64	3	PL Bank 64 VCCO (1.0 – 1.8V) sourced by the Carrier Cards.
VCCO_HP_65	3	PL Bank 65 VCCO (1.0 – 1.8V) sourced by the Carrier Cards.
VCCO_HD_47	3	PL Bank 47 VCCO (1.2 – 3.3V) sourced by the Carrier Cards.
VCCO_HD_48	3	PL Bank 48 VCCO (1.2 – 3.3V) sourced by the Carrier Cards.
MGTRAVCC	3	PS GTR Core Voltage (0.85V) sourced by the Carrier Cards.
MGTRAVTT	2	PS GTR Termination Voltage (1.8V) sourced by the Carrier Cards.
MGTAVCC	6	PL GTH Core Voltage (0.9V) sourced by the Carrier Cards.
MGTAVTT	6	PL GTH Termination Voltage (1.2V) sourced by the Carrier Cards.
MGTVCCAUX	2	PL GTH Auxiliary Voltage (1.8V) sourced by the Carrier Cards.
VCCO_PSIO_501	1	PS MIO Bank 501 VCCO (1.8/2.5/3.3V) sourced by the Carrier Cards.
PS_VBATT	1	PS VBATT Input (1.5V) sourced by the Carrier Cards.
MGTRAVCC_Sense, MGTRAVTT_Sense, MGTAVCC_Sense, MGTAVTT_Sense, MGTVCCAUX_Sense, VCCO_HP_64_Sense, VCCO_HP_65_Sense, VCCO_HD_47_Sense, VCCO_HD_48_Sense	9	Voltage Sense Feedback – These output pins are used by the custom Carrier Cards to compensate for the voltage loss across the JX connectors.
SOM_PG_OUT	1	SOM Power Good Output – This signal is used to enable the Carrier Card voltage regulators.
GND	156	Ground Pins
VIN	8	Main Input Voltage (5 to 12V DC).

4.1 PS MIO Interface

The PS MIO interface consists of 26 MIO pins, MIO[26:51] connected to the PS MIO bank 501. These MIO pins are routed to the JX3 connector and are available to the custom Carrier Cards. The PS bank 501 I/O is operated at 1.8V, 2.5V, or 3.3V provided by the custom Carrier Cards via JX3 connector. This full bank of MIO pins can be used on a custom Carrier Card to implement various interfaces (please refer to the Xilinx UG1085 for more information on the PS MIO available interfaces). On the Avnet UltraZed -EV Carrier Card, PS MIO bank 501 is operated at 3.3V and used to implement the following interfaces:

- microSD card
- Dual USB-UART ports
- PS PMOD header
- PS user LED
- PCIe Root Port Reset
- Display Port auxiliary interface

The following table shows the UltraZed-EV SOM PS MIO[26:51] pins available on the JX3 connector.

Table 9 – PS MIO Bank 501 Pin Assignments

Row/Column	JX3 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
20			MIO_40	
21	MIO_26		MIO_42	MIO_41
22	MIO_28	MIO_27	MIO_44	MIO_43
23	MIO_30	MIO_29		MIO_45
24		MIO_31	MIO_46	
25	MIO_32			MIO_47
26	MIO_34	MIO_33	MIO_48	
27	MIO_36	MIO_35		MIO_49
28		MIO_37	MIO_50	
29	MIO_38			MIO_51
30		MIO_39		

Please refer to the pages 3, 5, 12, 14, and 15 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on the PS MIO Interfaces implemented on the Avnet Carrier Card.

4.2 PS USB 2.0 Connector Interface

The UltraZed-EV SOM USB 2.0 ULPI PHY connector side interface can be used on a custom Carrier Card to implement a USB 2.0 interface using a USB/microUSB connector. If so desired, this USB 2.0 ULPI PHY connector side interface along with a SOM PS GTR transceiver (available on the JX3 connector) can be used to implement a USB 2.0/3.0 interface via a single USB 2.0/3.0 connector. The USB 2.0/3.0 interface can be designed to support Host/OTG or Device mode. The following table shows the UltraZed-EV SOM USB 2.0 ULPI PHY connector side interface pins available on the JX3 connector.

Table 10 – PS USB 2.0 Connector Interface Pin Assignments

Row/Column	JX3 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
14	USB_OTG_P			
15	USB_OTG_N			
16		USB_OTG_CPEN		
17	USB_ID	USB_OTG_VBUS		

Please refer to the page 16 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on the USB2.0/3.0 Interface implemented on the Avnet Carrier Card.

4.3 PS RJ45 Connector Interface

The UltraZed-EV SOM Gigabit Ethernet PHY connector side interface along with an RJ45 connector on the custom Carrier Card can be used to implement a single Gigabit Ethernet port. The following table shows the UltraZed-EV SOM Gigabit Ethernet PHY connector side interface pins available on the JX3 connector.

Table 11 – PS RJ45 Connector Interface Pin Assignments

Row/Column	JX3 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
14			ETH_MD1_P	
15			ETH_MD1_N	ETH_MD2_P
16				ETH_MD2_N
17			ETH_MD3_P	
18		ETH_PHY_LED1	ETH_MD3_N	ETH_MD4_P
19				ETH_MD4_N
20		ETH_PHY_LED0		

Please refer to the page 5 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on the RJ45 connector Interface implemented on the Avnet Carrier Card.

4.4 PS GTR Transceivers Interface

The UltraZed-EV SOM provides 4 PS GTR transceivers along with 4 GTR reference clock inputs to the custom Carrier Cards via the JX3 connector. These 4 transceivers can be used on a custom Carrier Card to implement USB 3.0, Display Port, SATA host, and PCIe interfaces. Please refer to the UG1085 (Zynq UltraScale+ Technical Reference Manual) for more information on how each GTR transceiver can be used in a design.

The GTR transceiver power (0.85V and 1.8V rails) must be supplied by the custom Carrier Card via JX3 connector. Please refer to the *Power Requirements* section of this document for more information. The following table shows the UltraZed-EV SOM PS GTR and GTR reference clock input pins available on the JX3 connector.

Table 12 – PS GTR Interface Pin Assignments

Row/Column	JX3 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
2	GTR_TX3_P		GTR_TX2_P	
3	GTR_TX3_N		GTR_TX2_N	
4		GTR_RX3_P		GTR_RX2_P
5		GTR_RX3_N		GTR_RX2_N
6	GTR_TX1_P		GTR_TX0_P	
7	GTR_TX1_N		GTR_TX0_N	
8		GTR_RX1_P		GTR_RX0_P
9		GTR_RX1_N		GTR_RX0_N
10	GTR_REFCLK3_P		GTR_REFCLK2_P	
11	GTR_REFCLK3_N		GTR_REFCLK2_N	
12		GTR_REFCLK1_P		GTR_REFCLK0_P
13		GTR_REFCLK1_N		GTR_REFCLK0_N

Please refer to the pages 3, 5, 7, and 16 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how PS GTR interfaces are implemented on the Avnet Carrier Card.

4.5 PL GTH Transceivers Interface

The UltraZed-EV SOM provides 16 PL GTH transceivers along with 8 GTH reference clock inputs to the custom Carrier Cards via the JX2 connector. These 16 transceivers can be used on a custom Carrier Card to implement variety of interfaces.

The GTH transceiver power (0.9V, 1.2V, and 1.8V rails) must be supplied by the custom Carrier Card via JX2 connector. Please refer to the *Power Requirements* section of this document for more information. The following table shows the UltraZed-EV SOM PL GTH and GTH reference clock input pins available on the JX2 connector.

Table 13 – PL GTH Interface Pin Assignments

Row/Column	JX2 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
20	GTH0_TX_P		GTH1_TX_P	
21	GTH0_TX_N	GTH0_RX_P	GTH1_TX_N	GTH1_RX_P
22		GTH0_RX_N		GTH1_RX_N
23	GTH2_TX_P		GTH3_TX_P	
24	GTH2_TX_N	GTH2_RX_P	GTH3_TX_N	GTH3_RX_P
25		GTH2_RX_N		GTH3_RX_N
26	GTH_REFCLK0_P		GTH4_TX_P	
27	GTH_REFCLK0_N	GTH_REFCLK1_P	GTH4_TX_N	GTH4_RX_P
28		GTH_REFCLK1_N		GTH4_RX_N
29	GTH5_TX_P		GTH6_TX_P	
30	GTH5_TX_N	GTH5_RX_P	GTH6_TX_N	GTH6_RX_P
31		GTH5_RX_N		GTH6_RX_N
32	GTH7_TX_P		GTH_REFCLK2_P	
33	GTH7_TX_N	GTH7_RX_P	GTH_REFCLK2_N	GTH_REFCLK3_P
34		GTH7_RX_N		GTH_REFCLK3_N
35	GTH8_TX_P		GTH9_TX_P	
36	GTH8_TX_N	GTH8_RX_P	GTH9_TX_N	GTH9_RX_P
37		GTH8_RX_N		GTH9_RX_N
38	GTH10_TX_P		GTH11_TX_P	
39	GTH10_TX_N	GTH10_RX_P	GTH11_TX_N	GTH11_RX_P
40		GTH10_RX_N		GTH11_RX_N
41	GTH_REFCLK4_P		GTH12_TX_P	
42	GTH_REFCLK4_N	GTH_REFCLK5_P	GTH12_TX_N	GTH12_RX_P
43		GTH_REFCLK5_N		GTH12_RX_N
44	GTH13_TX_P		GTH14_TX_P	
45	GTH13_TX_N	GTH13_RX_P	GTH14_TX_N	GTH14_RX_P
46		GTH13_RX_N		GTH14_RX_N
47	GTH15_TX_P		GTH_REFCLK6_P	
48	GTH15_TX_N	GTH15_RX_P	GTH_REFCLK6_N	GTH_REFCLK7_P
49		GTH15_RX_N		GTH_REFCLK7_N

Please refer to the pages 4, 6, 7, 8, and 9 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how PL GTH interfaces are implemented on the Avnet Carrier Card.

4.6 PL HD I/O Pins

The PL HD I/O interface consists of 48 HD (High Density) I/O pins connected to the Zynq UltraScale+ MPSoC banks 47 and 48. These pins are routed to the JX2 connector and can be used on custom Carrier Cards to implement various interfaces. The PL HD bank I/O pins can be operated at 1.2V – 3.3V. The VCCO voltage for the PL HD bank must be supplied by the custom Carrier Cards via JX1 connector. Please refer to the *Power Requirements* section of this document for more information.

Note: The Zynq UltraScale+ MPSoC HD banks do not support differential output (single-ended I/O or differential input with external termination only).

Please refer to the page 6, 8, 9, and 11 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how PL HD I/O pins are used on the Avnet Carrier Card.

4.7 PL HP I/O Pins

The PL HP I/O interface consists of 104 HP (High Performance) I/O pins connected to the Zynq UltraScale+ MPSoC banks 64 and 65. These pins are routed to the JX1 connector (as 48 differential pairs and 8 single-ended signals) and can be used on custom Carrier Cards to implement various interfaces. The PL HP banks I/O pins are operated at 1.0V – 1.8V. The VCCO voltages for the PL HP banks must be supplied by the custom Carrier Cards via JX1 connector. Please refer to the *Power Requirements* section of this document for more information.

Please refer to the pages 6, 9, 13, and 14 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how PL HP I/O pins are used on the Avnet Carrier Card.

4.8 PL SYSMON Interface

The PL SYSMON interface is connected to the bank 0 of the Zynq UltraScale+ MPSoC and consists of ***VP***, ***VN***, ***DXP***, and ***DXN*** pins. These pins are routed to the JX1 connector and can be used on custom Carrier Cards to implement low speed analog interface. The SYSMON supply voltages, VCCADC and VREF are provided on the UltraZed-EV SOM. If not used, the SYSMON signals can be left unconnected on the custom Carrier Card. The following table shows the UltraZed-EV SOM SYSMON interface pins available on the JX1 connector.

Table 14 – PL SYSMON Interface Pin Assignments

Row/Column	JX1 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
48		SYSMON_DX_N		
49	SYSMON_V_N	SYSMON_DX_P		
50	SYSMON_V_P			

Please refer to the page 17 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how PL SYSMON pins are used on the Avnet Carrier Card.

4.9 SOM Reset Input

The UltraZed-EV SOM can be reset via an active low reset signal from the Carrier Card (***SOM_RESET_IN_N***) connected to the JX1 connector. The ***SOM_RESET_IN_N*** signal can be used to reset the MPSoC device as well as all other device on the UltraZed-EV SOM. The ***SOM_RESET_IN_N*** is a 1.8V signal and it is pulled up to the 1.8V rail on the UltraZed-EV SOM. The ***SOM_RESET_IN_N*** signal must have a minimum pulse width of ***3xPS_CLK or 90ns***, required by the UltraZed-EV SOM.

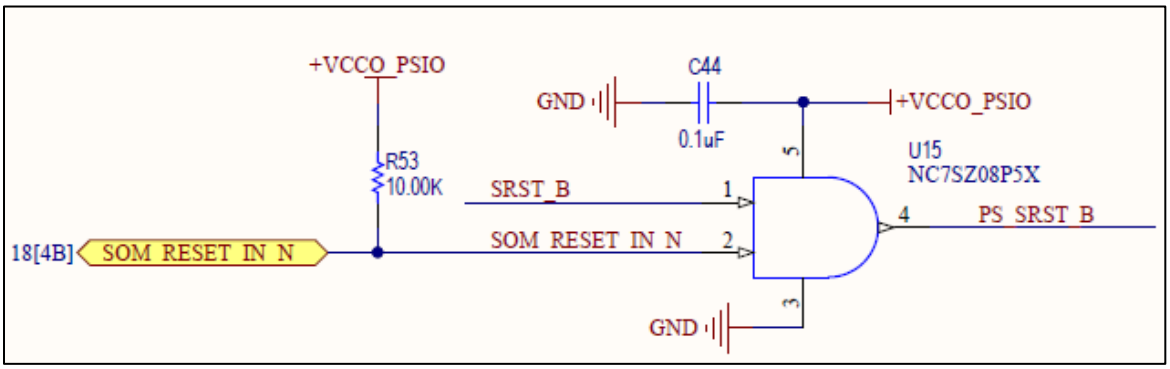


Figure 11 – SOM Input Reset Circuit on the UltraZed-EV SOM

Please refer to the page 13 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how SOM_RESET_IN_N signal is generated on the Avnet Carrier Card.

4.10 Carrier Card Reset Output

The UltraZed-EV SOM provides an ***active low*** reset signal to the Carrier Card (***CC_RESET_OUT_N***) via JX1 connector. The ***CC_RESET_OUT_N*** signal can be used to reset any device on the Carrier Card. The ***CC_RESET_OUT_N*** signal must be pulled up to 1.8V, 2.5V, or 3.3V on the custom Carrier Card.

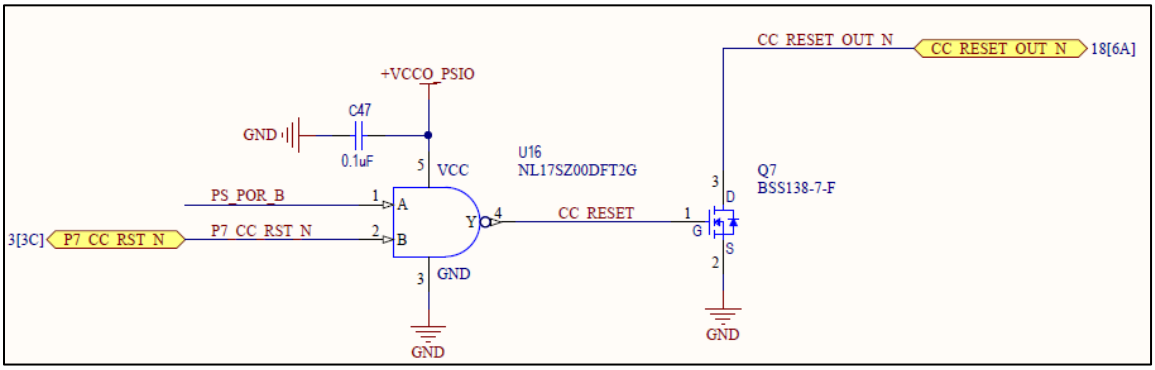


Figure 12 – Carrier Card Output Reset Circuit on the UltraZed-EV SOM

Please refer to the page 4 and 14 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how CC_RESET_OUT_N signals is used on the Avnet Carrier Card.

4.11 Carrier Card I2C Interface

The UltraZed-EV SOM provides a master I2C bus (***CC_SDA***, ***CC_SCL***, and ***CC_INT_N***) to the Carrier Card via the JX3 connector so that software can communicate with all I2C devices on the UltraZed-EV SOM as well as the slave I2C devices on the Carrier Card using a single I2C interface. The ***CC_SDA***, ***CC_SCL***, and ***CC_INT_N*** pins must be pulled up to the 1.8V, 2.5V, or 3.3V on the Carrier Card.

The Carrier Card I2C interface is connected to the channel 0 of the I2C 2-channel switch/mux device on the UltraZed-EV SOM. Carrier Cards can drive the ***INT0*** of the channel 0 via ***CC_INT_N***, if they so desire. The ***CC_INT_N*** signal is not specific to the I2C interface and can be used as a general-purpose interrupt from Carrie Cards to the UltraZed-EV SOM. If not used, the ***CC_INT_N*** signal must be pulled up to 1.8V, 2.5V, or 3.3V on the Carrier Card. Since channel 0 I2C bus is dedicated to the Carrier Card, I2C devices with any address can reside on this bus without conflicting with the I2C devices on the UltraZed-EV SOM. The following table shows the UltraZed-EV SOM Carrier Card I2C interface pins available on the JX3 connector.

Table 15 – Carrier Card I2C Interface Pin Assignments

Row/Column	JX3 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
1		CC_SDA		CC_SCL
19	CC_INT_N			

Please refer to the pages 4 and 5 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how Carrier Card I2C is used on the Avnet Carrier Card.

4.12 Ethernet MAC ID

A MAC Address device such as the Microchip ***24AA025E48T-I/OT*** device can be used on the custom Carrier Card. This device can be connected to the Carrier Card I2C interface (***CC_SDA*** and ***CC_SCL***).

Please refer to the page 5 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how the MAC ID is implemented on the Avnet Carrier Card.

4.13 JTAG Interface

Custom Carrier Cards must provide the JTAG interface to the UltraZed-EV SOM via JX1 connector. Carrier Cards can implement the JTAG interface using a JTAG header such as the Xilinx PC4 header, a USB-JTAG module such as the Digilent SMT2 module, or designing the JTAG interface using chip-down method on the Carrier Card. The JTAG interface on the custom Carrier Cards must be driven with 1.8V I/O standard.

The Avnet UltraZed-EV Carrier Card utilizes the Digilent SMT2 USB-JTAG module to interface to the UltraZed-EV SOM JTAG port. The Digilent USB-JTAG module VREF pin is connected to the 1.8V rail on the UltraZed-EV Carrier Card to provide 1.8V I/O on all JTAG signals. The following figure shows the JTAG interface on the Avnet UltraZed-EV Carrier Card.

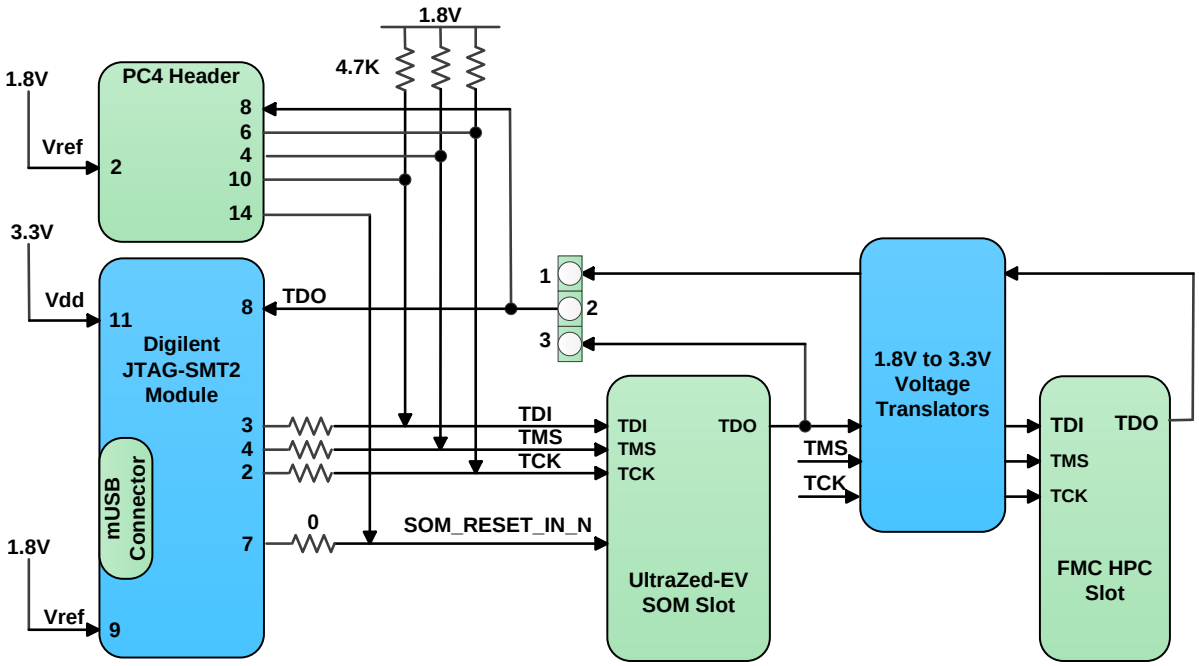


Figure 13 – Carrier Card JTAG Interface

The following table shows the UltraZed-EV SOM JTAG pins available on the JX1 connector.

Table 16 – PS JTAG Interface Pin Assignments

Row/Column	JX1 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
1	JTAG_TCK	JTAG_TMS		
2	JTAG_TDO	JTAG_TDI		

Please refer to the page 13 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on JTAG interface on the Avnet Carrier Card.

4.14 PMBus Interface

PMBus is used on the UltraZed-EV SOM to program/control/monitor all on-board PMBus voltage regulators. The UltraZed-EV SOM has access to the Carrier Card PMBus header via the JX1 connector (***PMBus_DATA***, ***PMBus_CLK***, and ***PMBus_ALERT_N*** signals). The Carrier Card PMBus header along with a programming dongle can be used to program all UltraZed-EV SOM PMBus voltage regulators.

An UltraZed-EV custom Carrier Card can provide a PMBus header for programming of all PMBus voltage regulators on the Carrier Card as well as the PMBus voltage regulators on the UltraZed-EV SOM, but it is not required to do so. The PMBus regulators on the UltraZed-EV SOM are pre-programmed prior to shipment. However, if programming of PMBus voltage regulators on a custom Carrier Card is required, the custom Carrier Card must implement the PMBus header.

After the initial programming of all PMBus voltage regulators, the UltraZed-EV SOM can drive the PMBus (via channel 1 of the I2C switch/mux and P5 port of the I2C 8-bit I/O expander) in order to control/monitor the PMBus voltage regulators on the UltraZed-EV SOM for the purpose of power management and/or measurements. If the PMBus is implemented on the custom Carrier Card, the UltraZed-EV SOM PMBus can monitor/control the Carrier Card PMBus voltage regulators as well. ***If not used, the UltraZed-EV SOM PMBus interface must be left unconnected on custom Carrier Cards so that the UltraZed-EV SOM can still control/monitor its on-board PMBus regulators***. The following figure shows how the PMBus is connected on the UltraZed-EV SOM and the Avnet UltraZed-EV Carrier Card.

Table 17 – PMBus Interface Pin Assignments

Row/Column	JX1 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
1			PMBus_SDA	PMBus_ALERT_N
2			PMBus_SCL	

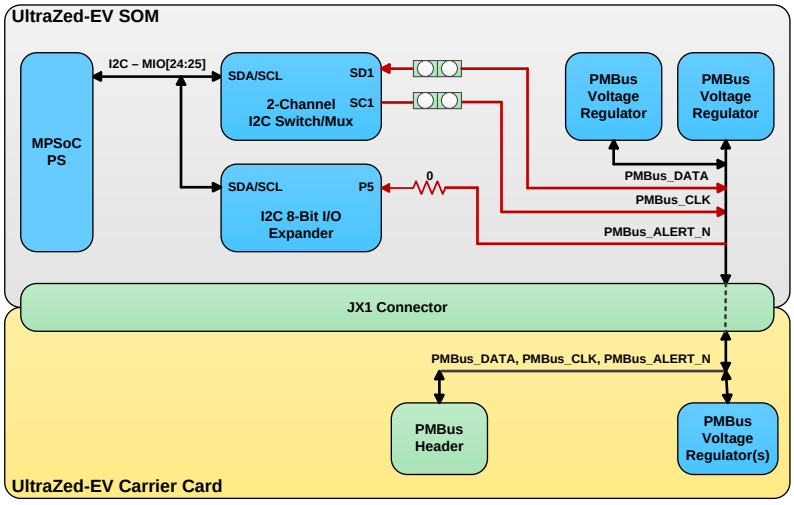


Figure 14 – PMBus Connections on the UltraZed-EV SOM and Carrier Card

Please refer to the page 17, 18, and 19 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how the PMBus interface is implemented on the Avnet Carrier Card.

4.15 Power Requirements

The UltraZed-EV SOM requires the following rails to be supplied by the Carrier Card. In return, the UltraZed-EV SOM will provide a voltage sense feedback for each rail (with the exception of the 5 – 12V input voltage and the PS MIO bank 501 VCCO) to the Carrier Card via JX3 connector (please refer to section 5 of this document for the JX1, JX2, and JX3 detail pinout information). The voltage sense feedback for each rail can be used by the regulator on the Carrier Card to compensate for the voltage loss across the JX connectors. Please refer to the DS925 (Zynq UltraScale+ MPSoC datasheet) for percent variation on all the following voltage rails when designing the power system for the custom Carrier Card. The custom Carrier Cards are required to supply the following rails to the UltraZed-EV SOM:

- 5 – 12V main input voltage via JX1 connector
- PS MGTRAVCC (0.85V) via JX3 connector
- PS MGTRAVTT (1.8V) via JX3 connector
- PL MGTAVCC (0.9V) via JX2 connector
- PL MGTAVTT(1.2V) via JX2 connector
- PL MGTVCCAUX (1.8V) via JX2 connector
- PS MIO bank 501 VCCO (1.8V, 2.5V, or 3.3V) via JX3 connector
- PL HP bank 64 VCCO (1.0V – 1.8V) via JX1 connector
- PL HP bank 65 VCCO (1.0V – 1.8V) via JX1 connector
- PL HD bank 47 VCCO (1.2V – 3.3V) via JX1 connector
- PL HD bank 48 VCCO (1.2V – 3.3V) via JX1 connector
- PS VBATT (1.5V) via JX3 connector

Table 18 – UltraZed-EV SOM Power Requirements

Voltage Rail Name	Voltage Value	Current Requirement	Voltage Sense Feedback
VIN	5 – 12V	11A @ 5V or 4.6A @ 12V	NA
MGTRAVCC	0.85V	1A	MGTRAVCC_Sense
MGTRAVTT	1.8V	1A	MGTRAVTT_Sense
MGTAVCC	0.90V	3A	MGTAVCC_Sense
MGTAVTT	1.2V	3A	MGTAVTT_Sense
MGTVCCAUX	1.8V	0.5A	MGTVCCAUX_Sense
VCCO_PSIO_501	1.8V, 2.5V, or 3.3V	0.5A	NA
VCCO_HP_64	1.0V – 1.8V	1A	VCCO_HP_64_Sense
VCCO_HP_65	1.0V – 1.8V	1A	VCCO_HP_65_Sense
VCCO_HD_47	1.2V – 3.3V	0.5A	VCCO_HD_47_Sense
VCCO_HD_48	1.2V – 3.3V	0.5A	VCCO_HD_48_Sense
PS_VBATT	1.5V	250nA	NA

Some of the above voltage rails can be combined to reduce the cost of power supply design on the custom Carrier Card. ***The MGTRAVCC, MGTRAVTT, MGTAVCC, MGTAVTT, and MGTVCCAUX analog voltage rails should not be combined with any VCCO rails***.

On the Avnet UltraZed-EV Carrier Card, all PL HP bank VCCOs are driven with a single 1.8V supply. The PL HD banks VCCO and PS MIO bank 501 VCCO are driven with a single 3.3V supply. The following lists the regulated voltage rails generated by PMBus voltage regulators on the UltraZed-EV Carrier Card for the UltraZed-EV SOM.

- 0.85V for the MGTRAVCC via JX3
- 1.8V for the MGTRAVTT via JX3
- 0.9V for the MGTAVCC via JX2
- 1.2V for the MGTAVTT via JX2
- 1.8V for the MGTVCCAUX via JX2
- 1.8V for all PL HP banks via JX1
- 3.3V for the PL HD banks and PS MIO bank 501 via JX1/JX3

4.16 Power Sequencing

Proper power sequencing is needed for the following rails supplied to the UltraZed-EV SOM by the Carrier Cards:

- PS MGTRAVCC
- PS MGTRAVTT
- PL MGTAVCC
- PL MGTAVTT
- PL MGTVCCAUX
- PS MIO bank 501 VCCO
- PL HP bank 64 VCCO
- PL HP bank 65 VCCO
- PL HD bank 47 VCCO
- PL HD bank 48 VCCO

The ***SOM_PG_OUT*** signal from the UltraZed-EV SOM (3.3V signal, connected to the JX1 connector) must be used to assist in power sequencing. The Carrier Card voltage regulator(s) should not be turned ON until the ***SOM_PG_OUT*** signal is asserted.

In order to boot from a device on the custom Carrier Card (such as booting from the microSD/SD Card), all power rails on the custom Carrier Card must be stable within 300ms of the ***SOM_PG_OUT*** assertion. This will ensure all custom Carrier Card power rails are up and stable before the ***PS_POR_B*** signal is de-asserted and the MPSoC boot execution is initiated on the UltraZed-EV SOM. The power rails on the Avnet UltraZed-EV Carrier Card are up and stable less than 100ms from the ***SOM_PG_OUT*** assertion.

Please refer to the page 14, 17, 18, and 19 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how the SOM_PG_OUT is used on the Avnet Carrier Card.

Once the ***SOM_PG_OUT*** signal is asserted, the Carrier Card must turn on the above voltage rails in the following sequence (the reverse sequence must be maintained on turn off):

1) PS MGTRAVCC rail followed by the PS MGTRAVTT rail.
2) PL MGTAVCC rail followed by the PL MGTAVTT rail and PL MGTVCCAUX rail.
3) PS bank 501 and PL banks 47, 48, 64, and 65 VCCO in any sequence after the MGTRAVCC/ MGTRAVTT/MGTAVCC/MGTAVTT/MGTVCCAUX rails.

4.17 Power Estimation Using XPE

Xilinx Power Estimator (XPE) should be used to generate worst case power estimations for selecting power devices for the I/O banks. The Xilinx Power Estimator (XPE) spreadsheet is available on Xilinx' website that can help you get started with your own power estimation. You may download this file and add or modify your desired PL utilization to provide a worst case estimation for your own VCCO supplies.

4.18 MPSoC Heat Sink with Fan

The UltraZed-EV SOM uses a heat sink with fan for the MPSoC device. Users can use either a 5V or a 12V fan with the UltraZed-EV SOM heat sink (The UltraZed-EV SOM is shipped with a 5V fan). The fan header are located on the UltraZed-EV custom Carrier Card and must be designed to match the fan voltage used on the SOM. Please refer to the *Carrier Card PCB Design Guideline* section of this document for more information.

NOTE: The heatsink with fan provided with the UltraZed-EV SOM is designed to be appropriate for most use cases except for the industrial high temperature extremes. It is expected that a system designer will perform worst case analysis of the thermal environment of the final solution and devise a proper thermal solution for the challenges presented in the operating environment.

Please refer to the page 17 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how the Fan Header is implemented on the Avnet Carrier Card.

5 UltraZed-EV SOM JX Micro Connectors

The UltraZed-EV SOM utilizes 3 micro headers to provide connections to the Carrier Card. ***Samtec SEAM8/SEAF8*** family connectors are used to implement the UltraZed-EV SOM to the Carrier Card connections (these connectors have 0.8mm pitch and are rated at up to 39Gbps data rate with 1.4A/pin current rating). The UltraZed-EV SOM will use a 120-pin (JX3, 4x30 pins) and two 200-pin (JX1 and JX2, 4x50 pins) connectors. These connectors will carry the following signals and power/ground pins (signal directions are with respect to the UltraZed-EV SOM):

JX1 Connector (200-pin Terminal, Samtec part number: SEAM8-50-S02.0-S-04-2-K)

- ***JTAG*** pins (***JTAG_TMS***, ***JTAG_TCK***, ***JTAG_TDI***, and ***JTAG_TDO***)
- ***SYSMON*** pins (***SYSMON_V_P***, ***SYSMON_V_N***, ***SYSMON_DX_P***, and ***SYSMON_DX_N)***
- 48 differential HP I/O pairs (***HP_DP***)
- 8 single ended signals (***HP_SE***)
- ***SOM_RESET_IN_N*** input
- ***CC_RESET_OUT_N*** output
- ***SOM_PG_OUT*** output
- PMBus signals (***PMBus_DATA***, ***PMBus_CLK***, and ***PMBus_ALERT_N***)
- Power and ground pins (***VCCO_HP_64***, ***VCCO_HP_65***, ***VCCO_HD_47***, ***VCCO_HD_48***, ***VIN*** and ***GND***)

JX2 Connector (200-pin Terminal, Samtec part number: SEAM8-50-S02.0-S-04-2-K)

- 48 single ended IO/24 differential input signals (***HD_SE***)
- 16 GTH transceivers (***GTH[0:15]***)
- 8 GTH reference clock inputs (***GTH_REFCLK[0:7]***)
- Power and ground pins (***MGTAVCC***, ***MGTAVTT***, ***MGTVCCAUX***, and ***GND***)

JX3 Connector (120-pin Terminal, Samtec part number: SEAM8-30-S02.0-S-04-2-K)

- ***PS GTR[0:3]***, ***PS GTR_REFCLK[0:3]***
- PS MIO bank 501 pins (***MIO[26:51]***)
- USB 2.0 connector interface (***USB_OTG_P***, ***USB_OTG_N***, ***USB_ID***, ***USB_OTG_VBUS***, and ***USB_OTG_CPEN***)
- Gigabit Ethernet connector interface (***ETH_MD[1:4]_P***, ***ETHMD[1:4]_N***, and ***ETH_PHY_LED[0:1]***)
- Carrier Card I2C interface (***CC_SDA***, ***CC_SCL***, and ***CC_INT_N***)
- ***PS_VBATT*** input
- Power and ground pins (***MGTRAVCC***, ***MGTRAVTT***, ***VCCO_PSIO_501***, and ***GND***)
- Voltage sense feedback output pins (***MGTAVCC_Sense***, ***MGTAVTT_Sense***, ***MGTVCCAUX_Sense,*** ***MGTRAVCC_Sense***, ***MGTRAVTT_Sense***, ***VCCO_HP_64_Sense***, ***VCCO_HP_65_Sense,*** ***VCCO_HD_47_Sense***, and ***VCCO_HD_48_Sense***)

5.1 Custom Carrier Cards Mating JX Receptacle Connectors

The JX1, JX2, and JX3 terminal connectors on the Avnet UltraZed-EV SOM have a default body height of 2mm. The body height of the SOM terminal connectors and the mating JX socket connectors for the custom Carrier Cards must be selected such that the ***Stack Height*** is <= 10mm when the UltraZed-EV is plugged onto the custom Carrier Card (this requirement must be met in order to meet the 16.375Gbps data rate for the PL GTH transceivers connected to the JX2 connector).

The Stack Height is calculated as follows:

Stack Height = Terminal Body Height(mm) + Socket Body Height(mm)

On the Avnet UltraZed-EV Carrier Card , the JX1, JX2, and JX3 socket connectors have 5mm body height:

JX1 Connector (200-pin Socket, Samtec part number: SEAF8-50-05.0-S-04-2-K)
JX2 Connector (200-pin Socket, Samtec part number: SEAF8-50-05.0-S-04-2-K)
JX3 Connector (120-pin Socket, Samtec part number: SEAF8-30-05.0-S-04-2-K)

So, the ***Stack Height*** when the Avnet UltraZed-EV SOM is plugged onto the Avnet UltraZed-EV Carrier Card would be:

2mm + 5mm = 7mm

Note: Custom UltraZed-EV SOM with terminal body height of ***5mm*** can also be ordered (the default terminal body height is 2mm). This will increase the ***Stack Height*** on the custom Carrier Cards to a maximum of 10mm (5mm terminal + 5mm socket = 10mm), if needed.

The following table summarizes connections to the UltraZed-EV SOM JX Micro Header Connectors.

Table 19 – UltraZed-EV SOM JX Micro Header Connectors Pinout Summary

SOM Connector	Signal Name	ZU7EV Bank	Voltage Domain
JX1	HP_DP_[00:23]_P/N, HP_SE_[00:03], VCCO_HP_64	64	VCCO_HP_64
	HP_DP_[24:47]_P/N, HP_SE_[04:07], VCCO_HP_65	65	VCCO_HP_65
	VCCO_HD_47	47	VCCO_HD_47
	VCCO_HD_48	48	VCCO_HD_48
	JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO	503	1.8V
	SYSMON_V_P, SYSMON_V_N, SYSMON_DX_P, SYSMON_DX_N	0	Please see Xilinx UG580 for more information.
	PMBus_DATA, PMBus_CLK, PMBus_ALERT_N	NA	3.3V
	SOM_RESET_IN_N		1.8V
	CC_RESET_OUT_N		Pulled up to 1.8V, 2.5V, or 3.3V on the Carrier Card
	VIN		5 – 12V
	SOM_PG_OUT		3.3V

JX2	GTH_TX[0:3]_P, GTH_TX[0:3]_N, GTH_RX[0:3]_P, GTH_RX[0:3]_N, GTH_REFCLK0_P, GTH_REFCLK0_N, GTH_REFCLK1_P, GTH_REFCLK1_N	227	MGTAVCC, MGTAVTT, MGTVCCAUX
	GTH_TX[4:7]_P, GTH_TX[4:7]_N, GTH_RX[4:7]_P, GTH_RX[4:7]_N, GTH_REFCLK2_P, GTH_REFCLK2_N, GTH_REFCLK3_P, GTH_REFCLK3_N	226	MGTAVCC, MGTAVTT, MGTVCCAUX
	GTH_TX[8:11]_P, GTH_TX[8:11]_N, GTH_RX[8:11]_P, GTH_RX[8:11]_N, GTH_REFCLK4_P, GTH_REFCLK4_N, GTH_REFCLK5_P, GTH_REFCLK5_N	225	MGTAVCC, MGTAVTT, MGTVCCAUX
	GTH_TX[12:15]_P, GTH_TX[12:15]_N, GTH_RX[12:15]_P, GTH_RX[12:15]_N, GTH_REFCLK6_P, GTH_REFCLK6_N, GTH_REFCLK7_P, GTH_REFCLK7_N	224	MGTAVCC, MGTAVTT, MGTVCCAUX
	MGTAVCC, MGTAVTT, MGTVCCAUX	224, 225, 226, and 227	MGTAVCC, MGTAVTT, MGTVCCAUX
	HD_SE_[00:11]	48	VCCO_HD_48
	HD_SE_[12:23]	47	VCCO_HD_47
JX3	GTR_TX[0:3]_P, GTR_TX[0:3]_N, GTR_RX[0:3]_P, GTR_RX[0:3]_N, GTR_REFCLK0_P, GTR_REFCLK0_N, GTR_REFCLK1_P, GTR_REFCLK1_N, GTR_REFCLK2_P, GTR_REFCLK2_N, GTR_REFCLK3_P, GTR_REFCLK3_N, MGTRAVCC, MGTRAVTT	505	MGTRAVCC, MGTRAVTT

	MIO_[26:51], VCCO_PSIO_501	501	VCCO_PSIO_501
	USB_OTG_P, USB_OTG_N, USB_ID, USB_OTG_VBUS, USB_OTG_CPEN	NA	1.8V
	ETH_MD[1:4]_P, ETHMD[1:4]_N, ETH_PHY_LED[0:1]		1.8V
	PS_VBATT		1.5V
	CC_SDA, CC_SCL, CC_INT_N		Pulled up to 1.8V, 2.5V, or 3.3V on the Carrier Card
	MGTRAVCC_Sense		MGTRAVCC
	MGTRAVTT_Sense		MGTRAVTT
	MGTAVCC_Sense		MGTAVCC
	MGTAVTT_Sense		MGTAVTT
	MGTVCCAUX_Sense		MGTVCCAUX
	VCCO_HP_64_Sense		VCCO_HP_64
	VCCO_HP_65_Sense		VCCO_HP_65
	VCCO_HD_47_Sense		VCCO_HD_47
	VCCO_HD_48_Sense		VCCO_HD_48

The JX1, JX2, and JX3 detail pinouts are shown in the following tables. In the following 3 tables:

- Pins in ***Red*** are Power, Ground, or Sense signals.
- Pins in ***Blue*** are dedicated signals.
- Pins in ***Black*** are multi-function/general-purpose pins.
- Pins in ***Black*** with _***GC*** designators are multi-function/general-purpose pins or Global Clock inputs.
- ***HP_DP*** stands for High Performance Differential Pairs, ***HP_SE*** stands for High Performance Single-Ended, and ***HD_SE*** stands for High Density Single-Ended

Table 20 – JX1 Connector Pin-out

Row/Column	Row D		Row C	
	Signal Name	ZU7EV Pin Number	Signal Name	ZU7EV Pin Number
1	JTAG_TCK	L19	JTAG_TMS	L21
2	JTAG_TDO	M20	JTAG_TDI	L20
3	VCCO_HP_65	AE1, AG7, AH10	VCCO_HP_65	AE1, AG7, AH10
4	VCCO_HP_65	AE1, AG7, AH10	HP_DP_01_P	AE18
5	HP_DP_00_P	AG18	HP_DP_01_N	AF18
6	HP_DP_00_N	AH18	GND	N/A
7	GND	N/A	HP_DP_05_P	AA16
8	HP_DP_04_P	AC17	HP_DP_05_N	AB16
9	HP_DP_04_N	AC18	GND	N/A
10	GND	N/A	HP_DP_09_P	AC16
11	HP_DP_08_P	AG16	HP_DP_09_N	AD16
12	HP_DP_08_N	AH16	GND	N/A
13	GND	N/A	GND	N/A
14	GND	N/A	HP_DP_13_GC_P	AD17
15	HP_DP_12_GC_P	AF16	HP_DP_13_GC_N	AE17
16	HP_DP_12_GC_N	AF17	GND	N/A
17	GND	N/A	GND	N/A
18	GND	N/A	HP_DP_17_P	AG13
19	HP_DP_16_P	AK13	HP_DP_17_N	AH13
20	HP_DP_16_N	AK12	GND	N/A
21	GND	N/A	HP_DP_21_P	AE14
22	HP_DP_20_P	AC14	HP_DP_21_N	AE13
23	HP_DP_20_N	AD14	GND	N/A
24	GND	N/A	HP_DP_25_P	AJ10
25	HP_DP_24_P	AF10	HP_DP_25_N	AK10
26	HP_DP_24_N	AG10	GND	N/A
27	GND	N/A	HP_DP_29_P	AK7
28	HP_DP_28_P	AJ5	HP_DP_29_N	AK6
29	HP_DP_28_N	AK5	GND	N/A
30	GND	N/A	GND	N/A
31	GND	N/A	HP_DP_33_GC_P	AH6
32	HP_DP_32_GC_P	AG6	HP_DP_33_GC_N	AJ6
33	HP_DP_32_GC_N	AG5	GND	N/A
34	GND	N/A	GND	N/A
35	GND	N/A	HP_DP_37_P	AJ4
36	HP_DP_36_P	AJ11	HP_DP_37_N	AK4

37	HP_DP_36_N	AK11	GND	N/A
38	GND	N/A	HP_DP_41_P	AG11
39	HP_DP_40_P	AH9	HP_DP_41_N	AH11
40	HP_DP_40_N	AJ9	GND	N/A
41	GND	N/A	HP_DP_45_P	AK3
42	HP_DP_44_P	AH3	HP_DP_45_N	AK2
43	HP_DP_44_N	AH2	VCCO_HD_48	E16, H15
44	VCCO_HD_47	D13, G12	VCCO_HD_48	E16, H15
45	VCCO_HD_47	D13, G12	VCCO_HD_48	E16, H15
46	VCCO_HD_47	D13, G12	CC_RESET_OUT_N	N/A
47	SOM_PG_OUT	N/A	GND	N/A
48	GND	N/A	SYSMON_DX_N	V14
49	SYSMON_V_N	U14	SYSMON_DX_P	V15
50	SYSMON_V_P	T15	VIN	N/A

Table 21 – JX1 Connector Pin-out (continued)

Row/Column	Row B		Row A	
	Signal Name	ZU7EV Pin Number	Signal Name	ZU7EV Pin Number
1	PMBus_SDA	N/A	PMBus_ALERT_N	N/A
2	PMBus_SCL	N/A	SOM_RESET_IN_N	N/A
3	VCCO_HP_64	AC15, AF14, AG17	VCCO_HP_64	AC15, AF14, AG17
4	VCCO_HP_64	AC15, AF14, AG17	HP_DP_03_P	AD19
5	HP_DP_02_P	AH17	HP_DP_03_N	AE19
6	HP_DP_02_N	AJ17	GND	N/A
7	GND	N/A	HP_DP_07_P	AK17
8	HP_DP_06_P	AJ16	HP_DP_07_N	AK18
9	HP_DP_06_N	AK16	GND	N/A
10	GND	N/A	HP_DP_11_P	AJ15
11	HP_DP_10_P	AJ14	HP_DP_11_N	AK15
12	HP_DP_10_N	AK14	GND	N/A
13	GND	N/A	GND	N/A
14	GND	N/A	HP_DP_15_GC_P	AF15
15	HP_DP_14_GC_P	AG14	HP_DP_15_GC_N	AG15
16	HP_DP_14_GC_N	AH14	GND	N/A
17	GND	N/A	GND	N/A
18	GND	N/A	HP_DP_19_P	AA15
19	HP_DP_18_P	AA13	HP_DP_19_N	AB15

20	HP_DP_18_N	AB13	GND	N/A
21	GND	N/A	HP_DP_23_P	AD15
22	HP_DP_22_P	AA14	HP_DP_23_N	AE15
23	HP_DP_22_N	AB14	GND	N/A
24	GND	N/A	HP_DP_27_P	AF12
25	HP_DP_26_P	AF8	HP_DP_27_N	AF11
26	HP_DP_26_N	AF7	GND	N/A
27	GND	N/A	HP_DP_31_P	AK9
28	HP_DP_30_P	AF6	HP_DP_31_N	AK8
29	HP_DP_30_N	AF5	GND	N/A
30	GND	N/A	GND	N/A
31	GND	N/A	HP_DP_35_GC_P	AG8
32	HP_DP_34_GC_P	AH7	HP_DP_35_GC_N	AH8
33	HP_DP_34_GC_N	AJ7	GND	N/A
34	GND	N/A	GND	N/A
35	GND	N/A	HP_DP_39_P	AF3
36	HP_DP_38_P	AJ2	HP_DP_39_N	AF2
37	HP_DP_38_N	AJ1	GND	N/A
38	GND	N/A	HP_DP_43_P	AE9
39	HP_DP_42_P	AH12	HP_DP_43_N	AE8
40	HP_DP_42_N	AJ12	GND	N/A
41	GND	N/A	HP_DP_47_P	AG4
42	HP_DP_46_P	AG1	HP_DP_47_N	AG3
43	HP_DP_46_N	AH1	VIN	N/A
44	VIN	N/A	HP_SE_04	AF1
45	HP_SE_00	AF13	HP_SE_05	AH4
46	HP_SE_01	AG19	VIN	N/A
47	VIN	N/A	HP_SE_06	AG9
48	HP_SE_02	AC13	HP_SE_07	AE10
49	HP_SE_03	AC19	VIN	N/A
50	VIN	N/A	VIN	N/A

Table 22 – JX2 Connector Pin-out

Row/Column	Row D		Row C	
	Signal Name	ZU7EV Pin Number	Signal Name	ZU7EV Pin Number
1	GND	N/A	MGTAVCC	A10, C10, F8, H8, M8, P8
2	HD_SE_00_P	B15	MGTAVCC	A10, C10, F8, H8, M8, P8
3	HD_SE_00_N	A15	HD_SE_01_P	A17
4	MGTAVCC	A10, C10, F8, H8, M8, P8	HD_SE_01_N	A16
5	HD_SE_04_GC_P	G16	GND	N/A
6	HD_SE_04_GC_N	G15	HD_SE_05_GC_P	E15
7	MGTAVCC	A10, C10, F8, H8, M8, P8	HD_SE_05_GC_N	D15
8	HD_SE_08_P	D16	GND	N/A
9	HD_SE_08_N	C16	HD_SE_09_P	J15
10	MGTAVCC	A10, C10, F8, H8, M8, P8	HD_SE_09_N	J14
11	HD_SE_12_P	B12	GND	N/A
12	HD_SE_12_N	A12	HD_SE_13_P	A14
13	MGTAVCC	A10, C10, F8, H8, M8, P8	HD_SE_13_N	A13
14	HD_SE_16_GC_P	D14	GND	N/A
15	HD_SE_16_GC_N	C13	HD_SE_17_GC_P	E14
16	GND	N/A	HD_SE_17_GC_N	E13
17	HD_SE_20_P	D12	GND	N/A
18	HD_SE_20_N	C12	HD_SE_21_P	H13
19	GND	N/A	HD_SE_21_N	H12
20	GTH0_TX_P	D6	GND	N/A
21	GTH0_TX_N	D5	GTH0_RX_P	D2
22	GND	N/A	GTH0_RX_N	D1
23	GTH2_TX_P	B6	GND	N/A
24	GTH2_TX_N	B5	GTH2_RX_P	B2
25	GND	N/A	GTH2_RX_N	B1
26	GTH_REFCLK0_P	D10	GND	N/A
27	GTH_REFCLK0_N	D9	GTH_REFCLK1_P	B10
28	GND	N/A	GTH_REFCLK1_N	B9
29	GTH5_TX_P	G8	GND	N/A
30	GTH5_TX_N	G7	GTH5_RX_P	G4
31	GND	N/A	GTH5_RX_N	G3

32	GTH7_TX_P	E8	GND	N/A
33	GTH7_TX_N	E7	GTH7_RX_P	E4
34	GND	N/A	GTH7_RX_N	E3
35	GTH8_TX_P	P6	GND	N/A
36	GTH8_TX_N	P5	GTH8_RX_P	N4
37	GND	N/A	GTH8_RX_N	N3
38	GTH10_TX_P	L4	GND	N/A
39	GTH10_TX_N	L3	GTH10_RX_P	K2
40	GND	N/A	GTH10_RX_N	K1
41	GTH_REFCLK4_P	L8	GND	N/A
42	GTH_REFCLK4_N	L7	GTH_REFCLK5_P	J8
43	GND	N/A	GTH_REFCLK5_N	J7
44	GTH13_TX_P	V6	GND	N/A
45	GTH13_TX_N	V5	GTH13_RX_P	U4
46	GND	N/A	GTH13_RX_N	U3
47	GTH15_TX_P	R4	GND	N/A
48	GTH15_TX_N	R3	GTH15_RX_P	P2
49	GND	N/A	GTH15_RX_N	P1
50	GND	N/A	GND	N/A

Table 23 – JX2 Connector Pin-out (continued)

Row/Column	Row B		Row A	
	Signal Name	ZU7EV Pin Number	Signal Name	ZU7EV Pin Number
1	GND	N/A	MGTAVTT	A6, B8, C6, D8, E6, G6, J6, L6, N6, R6, U6
2	HD_SE_02_P	J16	MGTAVTT	A6, B8, C6, D8, E6, G6, J6, L6, N6, R6, U6
3	HD_SE_02_N	H16	HD_SE_03_P	K15
4	MGTAVTT	A6, B8, C6, D8, E6, G6, J6, L6, N6, R6, U6	HD_SE_03_N	K14
5	HD_SE_06_GC_P	F16	MGTVCCAUX	E10, G10
6	HD_SE_06_GC_N	F15	HD_SE_07_GC_P	E17
7	MGTAVTT	A6, B8, C6, D8, E6, G6, J6, L6, N6, R6, U6	HD_SE_07_GC_N	D17
8	HD_SE_10_P	C17	MGTVCCAUX	E10, G10
9	HD_SE_10_N	B16	HD_SE_11_P	L15

10	MGTAVTT	A6, B8, C6, D8, E6, G6, J6, L6, N6, R6, U6	HD_SE_11_N	L14
11	HD_SE_14_P	C14	GND	N/A
12	HD_SE_14_N	B14	HD_SE_15_P	H14
13	MGTAVTT	A6, B8, C6, D8, E6, G6, J6, L6, N6, R6, U6	HD_SE_15_N	G14
14	HD_SE_18_GC_P	G13	GND	N/A
15	HD_SE_18_GC_N	F13	HD_SE_19_GC_P	F12
16	GND	N/A	HD_SE_19_GC_N	E12
17	HD_SE_22_P	K13	GND	N/A
18	HD_SE_22_N	J12	HD_SE_23_P	K12
19	GND	N/A	HD_SE_23_N	K11
20	GTH1_TX_P	G8	GND	N/A
21	GTH1_TX_N	G7	GTH1_RX_P	C4
22	GND	N/A	GTH1_RX_N	C3
23	GTH3_TX_P	A8	GND	N/A
24	GTH3_TX_N	A7	GTH3_RX_P	A4
25	GND	N/A	GTH3_RX_N	A3
26	GTH4_TX_P	H6	GND	N/A
27	GTH4_TX_N	H5	GTH4_RX_P	H2
28	GND	N/A	GTH4_RX_N	H1
29	GTH6_TX_P	F6	GND	N/A
30	GTH6_TX_N	F5	GTH6_RX_P	F2
31	GND	N/A	GTH6_RX_N	F1
32	GTH_REFCLK2_P	H10	GND	N/A
33	GTH_REFCLK2_N	H9	GTH_REFCLK3_P	F10
34	GND	N/A	GTH_REFCLK3_N	F9
35	GTH9_TX_P	M6	GND	N/A
36	GTH9_TX_N	M5	GTH9_RX_P	M2
37	GND	N/A	GTH9_RX_N	M1
38	GTH11_TX_P	K6	GND	N/A
39	GTH11_TX_N	K5	GTH11_RX_P	J4
40	GND	N/A	GTH11_RX_N	J3
41	GTH12_TX_P	W4	GND	N/A
42	GTH12_TX_N	W3	GTH12_RX_P	V2
43	GND	N/A	GTH12_RX_N	V1
44	GTH14_TX_P	T6	GND	N/A
45	GTH14_TX_N	T5	GTH14_RX_P	T2
46	GND	N/A	GTH14_RX_N	T1

47	GTH_REFCLK6_P	R8	GND	N/A
48	GTH_REFCLK6_N	R7	GTH_REFCLK7_P	N8
49	GND	N/A	GTH_REFCLK7_N	N7
50	GND	N/A	GND	N/A

Table 24 – JX3 Connector Pin-out

Row/Column	Row D		Row C	
	Signal Name	ZU7EV Pin Number	Signal Name	ZU7EV Pin Number
1	GND	N/A	CC_SDA	N/A
2	GTR_TX3_P	G25	GND	N/A
3	GTR_TX3_N	G26	GND	N/A
4	GND	N/A	GTR_RX3_P	G29
5	GND	N/A	GTR_RX3_N	G30
6	GTR_TX1_P	K27	GND	N/A
7	GTR_TX1_N	K28	GND	N/A
8	GND	N/A	GTR_RX1_P	J29
9	GND	N/A	GTR_RX1_N	J30
10	GTR_REFCLK3_P	H23	GND	N/A
11	GTR_REFCLK3_N	H24	GND	N/A
12	GND	N/A	GTR_REFCLK1_P	L25
13	GND	N/A	GTR_REFCLK1_N	L26
14	USB_OTG_P	N/A	GND	N/A
15	USB_OTG_N	N/A	GND	N/A
16	GND	N/A	USB_OTG_CPEN	N/A
17	USB_ID	N/A	USB_OTG_VBUS	N/A
18	VCCO_PSIO_501	B22, D23, E21	ETH_PHY_LED1	N/A
19	CC_INT_N	N/A	GND	N/A
20	MGTRAVCC_Sense	N/A	ETH_PHY_LED0	N/A
21	MIO_26	B20	PS_VBATT	U20
22	MIO_28	A21	MIO_27	B21
23	MIO_30	C21	MIO_29	D21
24	VCCO_HD_47_Sense	N/A	MIO_31	A22
25	MIO_32	G20	MGTRAVTT_Sense	N/A
26	MIO_34	B24	MIO_33	C22
27	MIO_36	D22	MIO_35	B23
28	VCCO_HD_48_Sense	N/A	MIO_37	F21
29	MIO_38	C23	VCCO_HP_65_Sense	N/A
30	VCCO_HP_64_Sense	N/A	MIO_39	E22

Table 25 – JX3 Connector Pin-out (continued)

Row/Column	Row B		Row A	
	Signal Name	ZU7EV Pin Number	Signal Name	ZU7EV Pin Number
1	GND	N/A	CC_SCL	N/A
2	GTR_TX2_P	J25	GND	N/A
3	GTR_TX2_N	J26	GND	N/A
4	GND	N/A	GTR_RX2_P	H27
5	GND	N/A	GTR_RX2_N	H28
6	GTR_TX0_P	M27	GND	N/A
7	GTR_TX0_N	M28	GND	N/A
8	GND	N/A	GTR_RX0_P	L29
9	GND	N/A	GTR_RX0_N	L30
10	GTR_REFCLK2_P	K23	GND	N/A
11	GTR_REFCLK2_N	K24	GND	N/A
12	GND	N/A	GTR_REFCLK0_P	M23
13	GND	N/A	GTR_REFCLK0_N	M24
14	ETH_MD1_P	N/A	GND	N/A
15	ETH_MD1_N	N/A	ETH_MD2_P	N/A
16	GND	N/A	ETH_MD2_N	N/A
17	ETH_MD3_P	N/A	GND	N/A
18	ETH_MD3_N	N/A	ETH_MD4_P	N/A
19	GND	N/A	ETH_MD4_N	N/A
20	MIO_40	C24	GND	N/A
21	MIO_42	E23	MIO_41	D24
22	MIO_44	E24	MIO_43	F22
23	MGTVCCAUX_Sense	N/A	MIO_45	F23
24	MIO_46	K20	MGTAVCC_Sense	N/A
25	MGTRAVTT	H25, K25, L27	MIO_47	K21
26	MIO_48	J21	GND	N/A
27	MGTRAVTT	H25, K25, L27	MIO_49	G21
28	MIO_50	J20	MGTAVTT_Sense	N/A
29	MGTRAVCC	J23, L23	MIO_51	H21
30	MGTRAVCC	J23, L23	MGTRAVCC	J23, L23

6 UltraZed-EV SOM Mechanical Dimensions

The following figure shows the UltraZed-EV SOM mechanical dimensions. UltraZed-EV SOM measures 2.50” x 4.00” (63.5 mm x 101.6 mm).

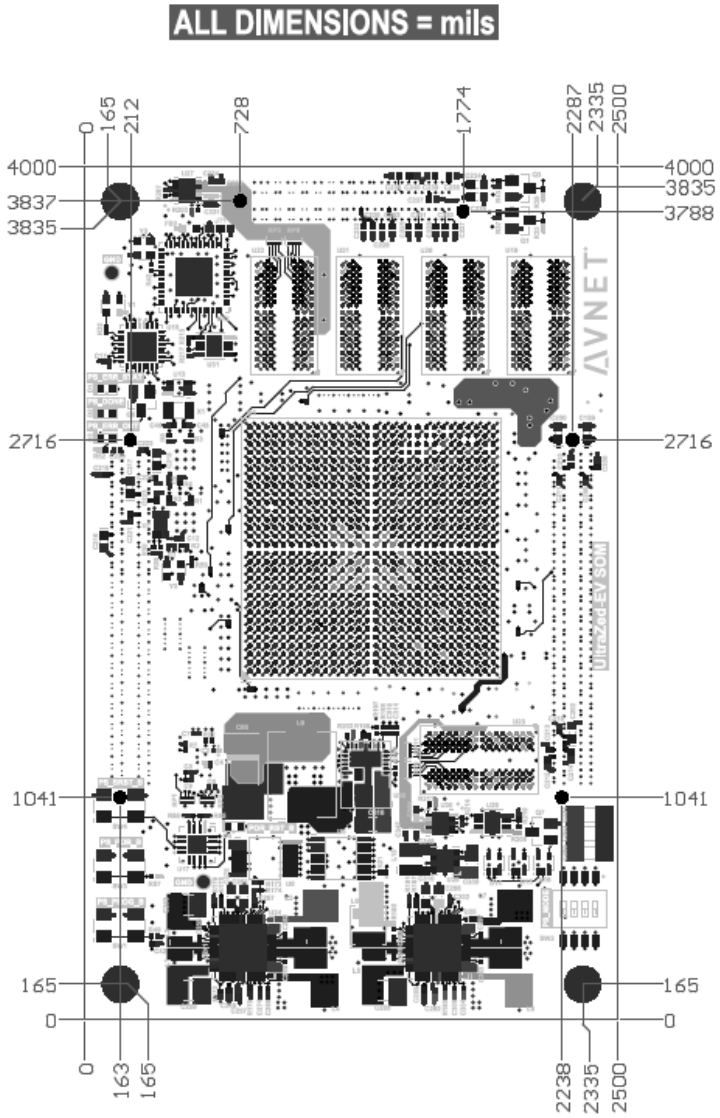


Figure 15 – UltraZed-EV SOM Mechanical Dimensions

7 Carrier Card PCB Design Guidelines

The following sections provide general PCB design guidelines for designing with the UltraZed-EV SOM. PCB design files for the Avnet UltraZed Carrier Cards are available upon request to assist you with your custom Carrier Card PCB design.

7.1 Connector Land and Alignment

It is extremely important that Carrier card designers ensure that the Micro Headers have the proper land patterns and that the connectors are aligned correctly. The land pattern is featured in the *Mechanical Considerations* section of this document. Connector alignment is ensured if the alignment pin holes in the PCB connector pattern are in the correct positions and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

Please refer to the UltraZed-EV SOM mechanical drawing available on the UltraZed-EV SOM documentation page www.ultrazed.org/product/ultrazed-EV for more information.

7.2 USB and Ethernet Connector Signal Routing

Due to critical timing that exists between the physical PHYs for the Gigabit Ethernet and USB2.0 interfaces to the associated PS controllers in the Xilinx Zynq MPSoC devices, Avnet has decided to implement the Gigabit Ethernet and USB 2.0 PHYs on the UltraZed-EV SOM. The outputs of the PHYs are connected to the JX3 connector. It is the responsibility of the custom Carrier Card designer to implement the proper connections to an RJ45 connector for Gigabit Ethernet and a USB connector for its USB2.0 interface. The following table depicts the necessary JX3 connections.

It is recommended that the Avnet UltraZed-EV Carrier Card design be used as an example and that the final solution are tailored to the specific custom Carrier Card requirements.

Table 26 – Carrier Card USB and Ethernet Connector Pins

Row/Column	JX3 Connector			
	Row D	Row C	Row B	Row A
	Signal Name			
14	USB_OTG_P	GND	ETH_MD1_P	GND
15	USB_OTG_N	GND	ETH_MD1_N	ETH_MD2_P
16	GND	USB_OTG_CPEN	GND	ETH_MD2_N
17	USB_ID	USB_OTG_VBUS	ETH_MD3_P	GND
18		ETH_PHY_LED1	ETH_MD3_N	ETH_MD4_P
19		GND	GND	ETH_MD4_N
20		ETH_PHY_LED0		GND

7.2.1 Ethernet Connector Pin routing

- ETH_MD1-4 differential pairs are to be routed 100Ω differential impedance.
- Length tune the differential signals to 10mils from longest to shortest.
- Length tune within a single pair (P and N) shall be length tuned to within 2mils of each other (P to N).

7.2.2 USB Connector Pin routing

- The USB differential pair is to be routed with 90Ω differential impedance.
- Length tune the differential signals to 10 mils from longest to shortest.
- Length tuning within a differential pair (P-to-N) shall be within 2 mils of each other (P to N).

7.3 PS GTR and PL GTH Transceiver Signal Routing

It is highly recommended that the guidelines described in the Xilinx document "UltraScale Architecture PCB Design" (UG583), and "UltraScale Architecture GTH Transceivers User Guide" (UG576) be reviewed prior to designing and routing GTR and GTH circuits. Here are some general guidelines that are followed on the UltraZed-EV SOM's GTR and GTH routing:

- All gigabit transceiver signals shall be routed as striplines.
- All Multi-Gigabit Transceiver TX, RX and related clock differential signals shall be routed differential at 100Ω differential impedance.
- Use 4x spacing between pairs.
- All Multi-Gigabit Transceiver differential signals can be treated as a group and shall be length tuned to within 10mils from the shortest pair to longest pair.
- All Multi-Gigabit Transceiver signals within a single pair (P and N) shall be length tuned to within 2 mils of each other (P to N).
- No More than two transitions (vias) are allowed for these signals.
- Multi-Gigabit Transceiver reference clocks do not need to be length tuned to the data signal pairs, but should be length tuned to each other within 10mils from the shortest pair to the longest pair.
- Multi-Gigabit Transceiver reference clock pairs must be tuned to within 2 mils (P to N).

The GTR and GTH transceiver routing on the Avnet UltraZed-EV Carrier Card should be used as reference for routing the GTRs and GTHs on a custom Carrier Card. Please refer to the UltraZed-EV Carrier Card ***PCB Layout Files*** on the www.ultrazed.org/product/ultrazed-ev-carrier-card website for more information. User should also use Signal Integrity (SI) analysis prior to fabricating the custom Carrier Card PCB. Avnet used *Avid Technologies* SI analysis services (www.avid-tech.com) to achieve the desired GTR and GTH performance on the Avnet UltraZed-EV SOM and Carrier Card.

7.4 PS MIO Routing

The routing of the PS MIO signals on the custom Carrier Cards depends on how these signals are defined and used. The PS MIO pins can be used to implement the following interfaces on the custom Carrier Cards:

- SD/microSD Card
- UART
- SPI
- I2C
- GPIO
- CAN

When routing the PS MIO signals, they should be length matched within each interface type. The following states general guidelines for routing the PS MIO signals on the custom Carrier Card.

- All signals are to be routed 50Ω characteristic impedance.

7.5 PL Single-Ended and Differential Signal Routing

The following states general guidelines for routing the PL single-ended and differential signal routing on the custom Carrier Card.

- All single ended signals are to be routed 50Ω characteristic impedance.
- The differential pairs are to be routed with 100Ω differential impedance.

The following table should be used when routing the PL single-ended and/or differential signals on the custom Carrier Cards. This table shows the routed net length (trace + the MPSoC package delay) for all PL signals connected from the MPSoC device to the JX1/JX2 connectors on the UltraZed-EV SOM. The JX1/JX2 signals are divided into groups and traces are length matched within each group. Since not all PL signals are routed to the JX1/JX2 connectors using equal trace length, trace length matching must be done on the custom Carrier Cards when an interface uses multiple signal groups. Please refer to the *JX1, JX2, and JX3 Routed Net Length* section of this document for more information.

Table 27 – UltraZed-EV SOM JX1/JX2 Routed Net Length

	Signal Group	UltraZed-EV Net Names	Average Routed Net Length (mils) (Trace + Package Delay)	MPSoC PL Bank
JX1 Connector	Group 1	HP_DP_[00:03]_P/N	1806.75	64
	Group 2	HP_DP_[04:07]_P/N	1625.86	64
	Group 3	HP_DP_[08:09]_P/N, HP_DP_[12:13]_P/N	1444.36	64
	Group 4	HP_DP_[10:11]_P/N; HP_DP_[14:15]_P/N	1537.26	64
	Group 5	HP_DP_[16:19]_P/N	1536.41	64
	Group 6	HP_DP_[20:23]_P/N	1735.15	64
	Group 7	HP_SE_[00:03]	2636.36	64
	Group 8	HP_DP_[24:27]_P/N	1636.76	65
	Group 9	HP_DP_[28:31]_P/N	1731.05	65
	Group 10	HP_DP_[32:33]_P/N, HP_DP_[36:37]_P/N	1736.78	65
	Group 11	HP_DP_[34:35]_P/N; HP_DP_[38:39]_P/N	1953.06	65
	Group 12	HP_DP_[40:43]_P/N	1971.77	65
	Group 13	HP_DP_[44:47]_P/N	2077.04	65
	Group 14	HP_SE_[04:07]	2220.65	65
JX2 Connector	Group 1	HD_SE_[00:03]_P/N	1964.13	48
	Group 2	HP_ SE_[04:07]_P/N	1943.30	48
	Group 3	HP_ SE_[08:11]_P/N	2068.35	48
	Group 4	HP_ SE_[12:15]_P/N	1829.88	47
	Group 5	HP_ SE_[16:19]_P/N	1707.12	47
	Group 6	HP_ SE_[20:23]_P/N	1970.00	47

7.6 JTAG Interface Signal Routing

The four dedicated JTAG signals are routed to the JX1 connector. A custom Carrier Card must utilize these JTAG signals in order to program and debug with the UltraZed-EV as a JTAG programming header is not implemented on UltraZed-EV SOM. When connecting additional JTAG devices in-line with the UltraZed-EV, be sure that TCK and TMS are properly buffered.

7.7 PL SYSMON Signal Routing

The PL SYSMON interface is connected to the bank 0 of the Zynq UltraScale+ MPSoC and consists of ***VP***, ***VN***, ***DXP***, and ***DXN*** pins. These pins are routed to the JX1 connector and can be used on custom Carrier Cards to implement low speed analog interface. The SYSMON supply voltages, VCCADC and VREF are provided on the UltraZed-EV SOM. Here are some general guidelines for designing the SYSMON interface on the custom Carrier Cards.

- Use 4X spacing on the traces.
- Single ended impedance is 50Ω and differential is 100Ω.
- All paired signals should be routed to within 50mils of each other.
- All interface signals should be routed to within 100mils of each other.

7.8 VIN Decoupling Caps

Please refer to page 18 of the Avnet UltraZed-EV Carrier Card schematics at the end of this document for information on the VIN decoupling cap requirements.

7.9 Mechanical Considerations

UltraZed-EV SOM measures 2.50” x 4.00” (63.5 mm x 101.6 mm). Custom Carrier Cards would have to be large enough to support the dimension shown in the *UltraZed-EV SOM Mechanical Dimensions* section of this document. The following figure is referenced as the footprint on a customer Carrier Card top view.

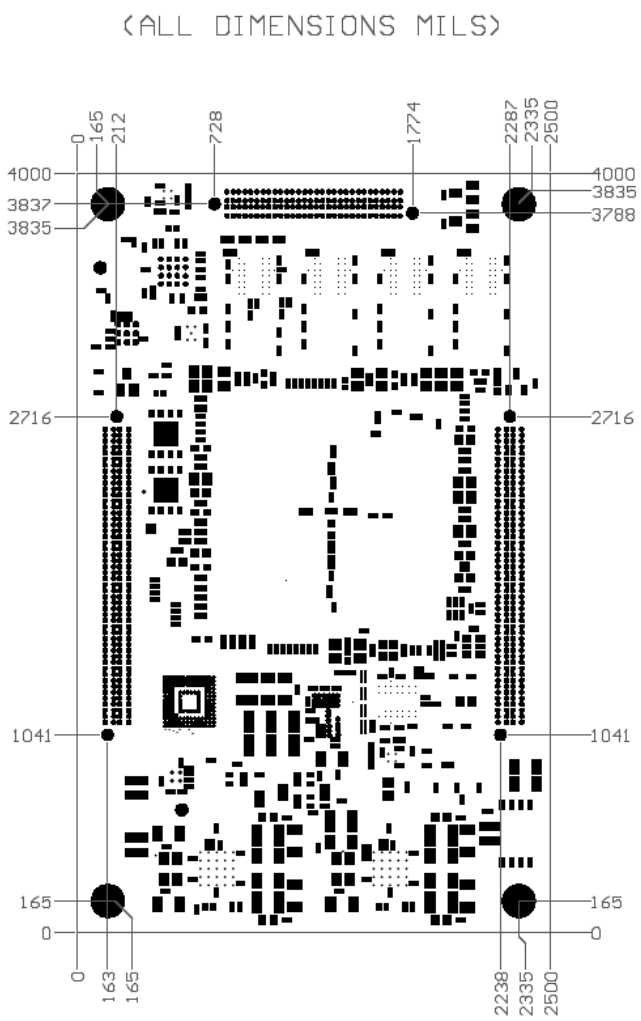


Figure 16 – UltraZed-EV SOM Top View Mechanical Dimensions

The UltraZed-EV SOM has a maximum vertical dimension of 0.607” (15.42 mm).

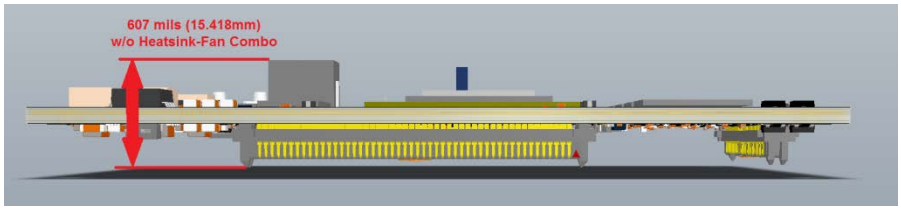


Figure 17 – UltraZed-EV SOM Side View Mechanical Dimensions

The UltraZed-EV SOM is delivered with an active fan (10.0 mm) and heatsink (14.5 mm) combination that has a vertical dimension of 965 mils (24.5 mm). The heatsink is available in a three other vertical sizes (9.5 mm, 19.5 mm, and 24.5 mm). The fan is available in a two other vertical sizes (6.9 mm and 15.0 mm).

NOTE: The heatsink with fan provided with the UltraZed-EV SOM is designed to be appropriate for most use cases except for the industrial high temperature extremes. It is expected that a system designer will perform worst case analysis of the thermal environment of the final solution and devise a proper thermal solution for the challenges presented in the operating environment.

The fan delivered with the UltraZed-EV SOM is designed to provide good thermal performance in a vertical size that is less than 1000 mils. The vertical dimension of the combination of the fan, heatsink, PCB, and connectors is 1333 mils (33.86 mm) and is documented below.

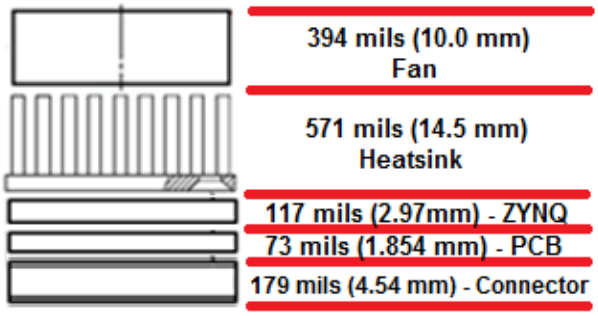


Figure 18 – UltraZed-EV SOM Overall Vertical Dimensions

The minimum vertical dimension of the fan and heatsink combination using the smallest heatsink and smallest fan is 646 mils (16.4 mm) and the maximum vertical dimension of the fan and heatsink combination using the largest heatsink and largest fan is 1555 mils (39.5 mm).

Figure 30 – UltraZed-EV SOM Fan and Heatsink MIN/MAX Combinations

NOTE: The above figures do not show the additional hardware required to bolt the fan to the heatsink. This additional hardware coincides with additional height to the solution accounting for the head of the screw.

7.10 Thermal Considerations

Thermal relief is an important design factor in each UltraZed-EV-based system design. A detailed thermal analysis should be performed for each specific application of UltraZed-EV and a customer designed Carrier Card. In support of this, UltraZed-EV has many design features to help dissipate heat from a system level.

The first feature is the fan. The UltraZed-EV SOM is shipped with an active heat sink/fan. The fan header must be placed on the custom Carrier Card and provide +5V to the UltraZed-EV SOM fan.

For maximum heat dissipation, any system airflow should pass parallel to the surface of the Zynq MPSoC device.

NOTE: The heatsink with fan provided with the UltraZed-EV SOM is designed to be appropriate for most use cases except for the industrial high temperature extremes. It is expected that a system designer will perform worst case analysis of the thermal environment of the final solution and devise a proper thermal solution for the challenges presented in the operating environment.

Please refer to page 17 of the Avnet UltraZed-EV Carrier Card schematic at the end of this document for more information on how the Fan Header is implemented on the Avnet UltraZed-EV Carrier Card.

Lastly, the four mounting holes on the four corners of UltraZed-EV are electrically connected to a heavier ground plane. With the additional mounting holes added to UltraZed-EV, system designers may choose to attach UltraZed-EV to their custom Carrier Card using metal standoff providing another path for heat dissipation.

Depending on the end-user application, the performance of the UltraZed-EV SOM will require a thermal solution to ensure expected performance across all temperature ranges.

The UltraZed-EV SOM comes with an example thermal solution of a Heatsink and Fan assembly. This active arrangement is secured directly to the Zynq UltraScale+ MPSoC via thermal tape and a 31mm clip solution that is pre-secured to the Zynq UltraScale+ device. A 24.5mm Tall Heat Sink and Sunon 5V DC Fan (PN: **MC30100V1-000U-A99**) solution are assembled and shipped with the UltraZed-EV SOM.

The active heat sink is powered by connecting a three position connector to the 5V fan mating connector on an end-user carrier card. This 3-pin keyed connector is .100” pitch and has the 5V conductor as pin 2 on the connector. For reference, the fan supplied with the UltraZed-EV SOM mates with the fan header on the UltraZed-EV Carrier Card.

Under most circumstances this Heatsink and Fan assembly should provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-users thermal environment and the possible enclosure of the UltraZed-EV SOM. For aggressive applications it is recommended that an accurate worst-case power analysis be performed in order to avoid the pitfalls of over designing or under designing your product’s power and thermal management system.

NOTE: End users should design a custom Heatsink and Fan assembly that are more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system.

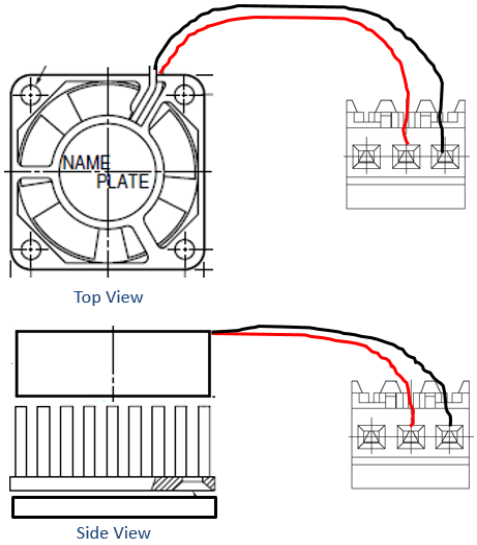


Figure 19 – Avnet 5VDC HeatSink and Fan Assembly

8 Getting Help and Support

If additional support is required, Avnet has many avenues to search depending on your needs. For general question regarding UltraZed-EV SOM and Carrier Card or accessories, please visit our website at www.ultrazed.org/product/ultrazed-EV. Here you can find documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding UltraZed-EV SOM hardware design, software application development, using Xilinx tools, training and other topics can be posted on the UltraZed-EV Support Forums at http://www.picozed.org/forums/zed-english-forum. Avnet's technical support team monitors the forum during normal business hours.

Those interested in customer-specific options on UltraZed-EV SOM can send inquiries to customize@avnet.com.

9 JX1, JX2, and JX3 Routed Net Lengths

The following tables show the routed net length from the Zynq UltraScale+ MPSoC device to the JX1, JX2, and JX3 connectors on the UltraZed-EV SOM.

Table 28 – JX1 Connector Routed Net Length

Net Name	IO Bank	Average Package Delay (mils)	PCB Trace Length (mils)	SOM Total Trace Length (mils)
HP_SE_00	64	729.62	1906.669	2636.29
HP_SE_01	64	746.13	1890.441	2636.57
HP_SE_02	64	616.75	2019.604	2636.36
HP_SE_03	64	594.13	2042.102	2636.24
HP_SE_04	65	1122.61	1098.18	2220.79
HP_SE_05	65	1080.84	1140.049	2220.89
HP_SE_06	65	881.00	1339.12	2220.12
HP_SE_07	65	762.16	1458.614	2220.78
HP_DP_00_N	64	795.12	1011.692	1806.81
HP_DP_00_P	64	803.73	1003.193	1806.93
HP_DP_01_N	64	675.68	1131.082	1806.76
HP_DP_01_P	64	673.04	1133.831	1806.87
HP_DP_02_N	64	774.18	1032.692	1806.87
HP_DP_02_P	64	761.06	1044.845	1805.90
HP_DP_03_N	64	706.29	1100.679	1806.97
HP_DP_03_P	64	714.71	1092.172	1806.88
HP_DP_04_N	64	547.00	1078.649	1625.65
HP_DP_04_P	64	547.14	1079.104	1626.25
HP_DP_05_N	64	656.13	969.719	1625.85
HP_DP_05_P	64	656.79	968.606	1625.40
HP_DP_06_N	64	792.37	833.188	1625.56
HP_DP_06_P	64	789.19	836.419	1625.61
HP_DP_07_N	64	835.19	790.472	1625.66
HP_DP_07_P	64	838.27	788.616	1626.89
HP_DP_08_N	64	788.68	655.386	1444.07
HP_DP_08_P	64	791.97	652.164	1444.14
HP_DP_09_N	64	549.04	895.524	1444.57
HP_DP_09_P	64	552.92	891.638	1444.56
HP_DP_10_N	64	743.31	794.054	1537.36
HP_DP_10_P	64	730.60	806.641	1537.24
HP_DP_11_N	64	717.90	819.739	1537.64
HP_DP_11_P	64	718.23	819.364	1537.60
HP_DP_12_GC_N	64	671.38	773.468	1444.84

HP_DP_12_GC_P	64	675.23	768.98	1444.21
HP_DP_13_GC_N	64	566.14	877.383	1443.52
HP_DP_13_GC_P	64	573.18	871.765	1444.95
HP_DP_14_GC_N	64	713.52	823.044	1536.56
HP_DP_14_GC_P	64	721.18	815.946	1537.13
HP_DP_15_GC_N	64	735.08	802.195	1537.28
HP_DP_15_GC_P	64	730.90	806.385	1537.29
HP_DP_16_N	64	811.75	724.87	1536.62
HP_DP_16_P	64	786.86	749.488	1536.35
HP_DP_17_N	64	701.56	834.609	1536.17
HP_DP_17_P	64	703.56	833.007	1536.56
HP_DP_18_N	64	555.87	980.715	1536.58
HP_DP_18_P	64	556.28	979.343	1535.63
HP_DP_19_N	64	552.46	984.03	1536.49
HP_DP_19_P	64	556.09	980.773	1536.86
HP_DP_20_N	64	554.49	1181.169	1735.66
HP_DP_20_P	64	553.95	1181.245	1735.20
HP_DP_21_N	64	720.25	1014.992	1735.25
HP_DP_21_P	64	700.87	1034.684	1735.55
HP_DP_22_N	64	564.26	1170.604	1734.87
HP_DP_22_P	64	565.73	1168.343	1734.08
HP_DP_23_N	64	565.88	1169.603	1735.49
HP_DP_23_P	64	557.36	1177.788	1735.15
HP_DP_24_N	65	781.72	854.267	1635.99
HP_DP_24_P	65	826.62	810.24	1636.86
HP_DP_25_N	65	870.46	766.495	1636.96
HP_DP_25_P	65	840.68	795.678	1636.35
HP_DP_26_N	65	883.54	753.426	1636.97
HP_DP_26_P	65	890.40	746.681	1637.08
HP_DP_27_N	65	817.03	820.123	1637.15
HP_DP_27_P	65	764.56	872.146	1636.71
HP_DP_28_N	65	1141.37	589.725	1731.10
HP_DP_28_P	65	1141.95	589.241	1731.19
HP_DP_29_N	65	1045.48	685.205	1730.68
HP_DP_29_P	65	1040.83	689.83	1730.66
HP_DP_30_N	65	996.64	734.148	1730.78
HP_DP_30_P	65	997.28	733.733	1731.01
HP_DP_31_N	65	935.56	796.026	1731.59
HP_DP_31_P	65	931.70	799.651	1731.35

HP_DP_32_GC_N	65	1009.24	727.935	1737.17
HP_DP_32_GC_P	65	1003.15	732.973	1736.12
HP_DP_33_GC_N	65	987.44	748.609	1736.05
HP_DP_33_GC_P	65	987.54	750.123	1737.66
HP_DP_34_GC_N	65	1002.68	950.151	1952.84
HP_DP_34_GC_P	65	1000.11	953.066	1953.18
HP_DP_35_GC_N	65	956.13	997.028	1953.16
HP_DP_35_GC_P	65	952.29	1000.012	1952.30
HP_DP_36_N	65	874.03	863.347	1737.38
HP_DP_36_P	65	870.75	865.925	1736.68
HP_DP_37_N	65	1080.31	656.246	1736.56
HP_DP_37_P	65	1071.11	665.483	1736.59
HP_DP_38_N	65	1226.73	726.904	1953.64
HP_DP_38_P	65	1205.02	747.006	1952.03
HP_DP_39_N	65	1146.78	807.202	1953.98
HP_DP_39_P	65	1128.50	824.852	1953.35
HP_DP_40_N	65	944.13	1026.948	1971.08
HP_DP_40_P	65	912.70	1059.753	1972.46
HP_DP_41_N	65	731.71	1240.776	1972.48
HP_DP_41_P	65	713.64	1257.606	1971.25
HP_DP_42_N	65	759.04	1212.167	1971.21
HP_DP_42_P	65	755.88	1214.775	1970.65
HP_DP_43_N	65	883.02	1089.629	1972.65
HP_DP_43_P	65	881.34	1091.049	1972.39
HP_DP_44_N	65	1169.90	906.7	2076.60
HP_DP_44_P	65	1172.48	904.618	2077.10
HP_DP_45_N	65	1200.68	876.024	2076.70
HP_DP_45_P	65	1196.33	881.064	2077.39
HP_DP_46_N	65	1163.05	914.392	2077.44
HP_DP_46_P	65	1144.21	932.251	2076.46
HP_DP_47_N	65	1146.38	930.605	2076.98
HP_DP_47_P	65	1147.73	929.887	2077.61

Table 29 – JX2 Connector Routed Net Length

Net Name	IO Bank	Average Package Delay (mils)	PCB Trace Length (mils)	SOM Total Trace Length (mils)
HD_SE_00_N	48	639.16	1325.113	1964.28
HD_SE_00_P	48	624.35	1340.428	1964.77
HD_SE_01_N	48	587.00	1377.348	1964.34
HD_SE_01_P	48	568.98	1395.226	1964.21
HD_SE_02_N	48	723.80	1239.851	1963.65
HD_SE_02_P	48	723.77	1241.395	1965.16
HD_SE_03_N	48	716.27	1247.093	1963.37
HD_SE_03_P	48	715.69	1247.599	1963.29
HD_SE_04_GC_N	48	719.70	1223.463	1943.16
HD_SE_04_GC_P	48	715.20	1227.981	1943.18
HD_SE_05_GC_N	48	646.11	1297.547	1943.66
HD_SE_05_GC_P	48	648.93	1294.784	1943.71
HD_SE_06_GC_N	48	721.68	1220.627	1942.31
HD_SE_06_GC_P	48	717.36	1226.39	1943.75
HD_SE_07_GC_N	48	496.69	1446.262	1942.95
HD_SE_07_GC_P	48	497.87	1445.813	1943.68
HD_SE_08_N	48	534.69	1534.457	2069.15
HD_SE_08_P	48	513.53	1554.486	2068.02
HD_SE_09_N	48	721.98	1346.054	2068.03
HD_SE_09_P	48	722.47	1345.051	2067.52
HD_SE_10_N	48	556.58	1512.62	2069.20
HD_SE_10_P	48	549.17	1519.236	2068.41
HD_SE_11_N	48	831.53	1236.457	2067.98
HD_SE_11_P	48	882.90	1185.58	2068.48
HD_SE_12_N	47	815.23	1014.029	1829.26
HD_SE_12_P	47	820.89	1007.351	1828.24
HD_SE_13_N	47	759.16	1070.613	1829.78
HD_SE_13_P	47	738.65	1092.158	1830.81
HD_SE_14_N	47	719.59	1110.839	1830.43
HD_SE_14_P	47	687.73	1142.107	1829.84
HD_SE_15_N	47	724.40	1106.349	1830.75
HD_SE_15_P	47	725.43	1104.5	1829.93
HD_SE_16_GC_N	47	737.61	970.242	1707.85
HD_SE_16_GC_P	47	733.93	973.352	1707.28
HD_SE_17_GC_N	47	675.23	1031.792	1707.02

HD_SE_17_GC_P	47	669.49	1037.684	1707.18
HD_SE_18_GC_N	47	725.53	981.69	1707.22
HD_SE_18_GC_P	47	723.97	983.257	1707.23
HD_SE_19_GC_N	47	742.10	965.125	1707.22
HD_SE_19_GC_P	47	736.45	969.497	1705.95
HD_SE_20_N	47	779.26	1191.224	1970.48
HD_SE_20_P	47	784.01	1185.465	1969.47
HD_SE_21_N	47	723.97	1246.354	1970.32
HD_SE_21_P	47	731.95	1237.345	1969.30
HD_SE_22_N	47	816.20	1153.208	1969.40
HD_SE_22_P	47	897.44	1073.417	1970.86
HD_SE_23_N	47	778.94	1191.804	1970.75
HD_SE_23_P	47	772.16	1197.24	1969.40
GTH0_TX_N	227	707.48	1136.39	1843.87
GTH0_TX_P	227	708.24	1136.42	1844.66
GTH0_RX_N	227	721.51	1122.07	1843.57
GTH0_RX_P	227	722.15	1122.10	1844.25
GTH1_TX_N	227	623.85	1219.31	1843.17
GTH1_TX_P	227	624.88	1219.34	1844.23
GTH1_RX_N	227	643.00	1200.38	1843.38
GTH1_RX_P	227	643.55	1200.17	1843.72
GTH2_TX_N	227	736.95	1107.41	1844.36
GTH2_TX_P	227	737.69	1106.86	1844.56
GTH2_RX_N	227	751.48	1091.74	1843.21
GTH2_RX_P	227	752.29	1091.77	1844.06
GTH3_TX_N	227	636.49	1206.42	1842.91
GTH3_TX_P	227	637.44	1206.92	1844.36
GTH3_RX_N	227	690.33	1155.48	1845.81
GTH3_RX_P	227	689.45	1153.80	1843.25
GTH_REFCLK0_N	227	600.37	1226.20	1826.57
GTH_REFCLK0_P	227	600.35	1226.23	1826.58
GTH_REFCLK1_N	227	657.75	1168.01	1825.75
GTH_REFCLK1_P	227	653.94	1174.42	1828.35
GTH4_TX_N	226	487.72	1383.48	1871.20
GTH4_TX_P	226	488.68	1382.25	1870.93
GTH4_RX_N	226	659.72	1212.09	1871.81
GTH4_RX_P	226	658.85	1211.77	1870.62
GTH5_TX_N	226	523.40	1346.76	1870.17
GTH5_TX_P	226	524.36	1346.40	1870.76

GTH5_RX_N	226	562.39	1308.49	1870.88
GTH5_RX_P	226	561.81	1308.95	1870.76
GTH6_TX_N	226	661.20	1208.83	1870.03
GTH6_TX_P	226	661.73	1208.62	1870.34
GTH6_RX_N	226	686.24	1184.86	1871.10
GTH6_RX_P	226	685.38	1185.26	1870.64
GTH7_TX_N	226	587.54	1282.94	1870.48
GTH7_TX_P	226	588.61	1283.42	1872.02
GTH7_RX_N	226	601.01	1270.77	1871.77
GTH7_RX_P	226	600.41	1270.56	1870.97
GTH_REFCLK2_N	226	503.95	1349.71	1853.67
GTH_REFCLK2_P	226	504.09	1349.74	1853.84
GTH_REFCLK3_N	226	546.75	1306.72	1853.47
GTH_REFCLK3_P	226	546.73	1306.75	1853.48
GTH8_TX_N	225	425.32	1879.14	2304.46
GTH8_TX_P	225	424.11	1879.17	2303.27
GTH8_RX_N	225	533.25	1771.55	2304.80
GTH8_RX_P	225	532.03	1771.51	2303.54
GTH9_TX_N	225	482.48	1821.89	2304.37
GTH9_TX_P	225	481.26	1821.69	2302.95
GTH9_RX_N	225	589.68	1713.84	2303.52
GTH9_RX_P	225	589.18	1713.87	2303.05
GTH10_TX_N	225	564.37	1739.62	2303.98
GTH10_TX_P	225	563.15	1741.49	2304.65
GTH10_RX_N	225	585.53	1718.20	2303.73
GTH10_RX_P	225	586.36	1718.00	2304.36
GTH11_TX_N	225	492.32	1811.87	2304.19
GTH11_TX_P	225	491.12	1811.73	2302.84
GTH11_RX_N	225	617.06	1687.29	2304.35
GTH11_RX_P	225	615.85	1687.39	2303.24
GTH_REFCLK4_N	225	495.97	1785.06	2281.03
GTH_REFCLK4_P	225	498.11	1782.58	2280.69
GTH_REFCLK5_N	225	485.20	1796.81	2282.01
GTH_REFCLK5_P	225	485.10	1797.21	2282.30
GTH12_TX_N	224	352.11	2040.11	2392.21
GTH12_TX_P	224	352.78	2039.65	2392.42
GTH12_RX_N	224	482.55	1910.62	2393.18
GTH12_RX_P	224	482.27	1910.77	2393.04
GTH13_TX_N	224	273.72	2118.47	2392.19

GTH13_TX_P	224	274.65	2119.05	2393.70
GTH13_RX_N	224	400.25	1992.63	2392.89
GTH13_RX_P	224	399.68	1992.56	2392.25
GTH14_TX_N	224	304.63	2088.32	2392.95
GTH14_TX_P	224	305.19	2087.93	2393.12
GTH14_RX_N	224	522.33	1869.99	2392.32
GTH14_RX_P	224	521.95	1869.95	2391.91
GTH15_TX_N	224	493.79	1899.93	2393.73
GTH15_TX_P	224	492.58	1899.26	2391.84
GTH15_RX_N	224	553.07	1839.27	2392.34
GTH15_RX_P	224	552.35	1839.93	2392.28
GTH_REFCLK6_N	224	412.71	1958.04	2370.75
GTH_REFCLK6_P	224	415.72	1955.69	2371.41
GTH_REFCLK7_N	224	452.75	1917.95	2370.70
GTH_REFCLK7_P	224	456.20	1914.69	2370.89

Table 30 – JX3 Connector Routed Net Length

Net Name	IO Bank	Average Package Delay (mils)	PCB Trace Length (mils)	SOM Total Trace Length (mils)
MIO_26	501	740.32	2690.482	3430.80
MIO_27	501	730.79	2700.003	3430.80
MIO_28	501	759.95	2670.289	3430.23
MIO_29	501	669.86	2760.601	3430.46
MIO_30	501	661.38	2769.432	3430.81
MIO_31	501	782.02	2648.11	3430.13
MIO_32	501	484.69	2945.733	3430.42
MIO_33	501	694.78	2736.5	3431.28
MIO_34	501	759.24	2672.186	3431.42
MIO_35	501	778.76	2651.55	3430.31
MIO_36	501	634.03	2796.22	3430.25
MIO_37	501	629.14	2801.126	3430.27
MIO_38	501	695.64	2734.556	3430.20
MIO_39	501	609.83	2820.464	3430.30
MIO_40	501	737.82	2692.781	3430.61
MIO_41	501	684.83	2745.958	3430.79
MIO_42	501	636.09	2794.384	3430.47
MIO_43	501	689.39	2741.244	3430.64
MIO_44	501	664.13	2766.292	3430.42
MIO_45	501	627.78	2802.244	3430.02
MIO_46	501	444.61	2986.032	3430.64
MIO_47	501	451.60	2978.836	3430.44
MIO_48	501	464.88	2965.505	3430.39
MIO_49	501	466.25	2964.553	3430.80
MIO_50	501	446.72	2983.858	3430.58
MIO_51	501	449.75	2980.996	3430.74
GTR_RX0_N	505	557.89	1478.881	2036.77
GTR_RX0_P	505	557.12	1479.308	2036.43
GTR_RX1_N	505	568.8	1468.068	2036.87
GTR_RX1_P	505	568.22	1468.223	2036.44
GTR_RX2_N	505	567.17	1468.612	2035.78
GTR_RX2_P	505	566.85	1470.829	2037.67
GTR_RX3_N	505	659.77	1377.409	2037.18
GTR_RX3_P	505	659.01	1378.182	2037.19

GTR_TX0_N	505	463.46	1745.42	2208.88
GTR_TX0_P	505	462.57	1745.723	2208.29
GTR_TX1_N	505	464.06	1745.013	2209.07
GTR_TX1_P	505	463.29	1745.823	2209.11
GTR_TX2_N	505	476.88	1730.826	2207.71
GTR_TX2_P	505	476.07	1732.999	2209.07
GTR_TX3_N	505	476.53	1732.194	2208.72
GTR_TX3_P	505	475.63	1732.442	2208.07
GTR_REFCLK0_N	505	385.44	1912.477	2297.92
GTR_REFCLK0_P	505	387.76	1909.987	2297.75
GTR_REFCLK2_N	505	430.36	1866.278	2296.64
GTR_REFCLK2_P	505	427.64	1869.438	2297.08
GTR_REFCLK1_N	505	404.35	1892.879	2297.23
GTR_REFCLK1_P	505	407.5	1890.156	2297.66
GTR_REFCLK3_N	505	488.22	1808.86	2297.08
GTR_REFCLK3_P	505	485.24	1811.799	2297.04

10 Avnet UltraZed-EV SOM Schematics

The Avnet UltraZed-EV SOM schematics are located on the UltraZed-EV documentation page.
You can locate that here: http://avnet.me/UltraZed-EV

11 Avnet UltraZed-EV Carrier Card Schematics

The Avnet UltraZed-EV Carrier Card schematics are located on the UltraZed-EV documentation page.
You can locate that here: http://avnet.me/UltraZed-EV