CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A070VW08 V2**
CUSTOMER APPROVED	Title : Name :

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 1.4)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.1.4)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 1.4)**

☐ **CUSTOMER REMARK :**

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Product Specification

7" COLOR TFT-LCD MODULE

MODEL NAME: A070VW08 V2

< >Preliminary Specification
< ◆ >Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0.0	2010/03/26	All	First Draft.
1.0	2011/02/17	5	Update Drawing
		4	Update Drawing
		10	Original 	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark	 |---|---|---|---|---|---|---| 	LED light bar Voltage	V_L	8.85	9.75	10.35	V	I_F=220mA	 	Power Consumption	P_{BL}	1.947	2.112	2.277	W	Note 1	 	LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3	 Note 1: The LED driving condition is defined for LED module (33LED). The voltage range will be 8.85V to 10.35V based on suggested driving current set as 220mA. Update 	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark	 |---|---|---|---|---|---|---| 	LED light bar Voltage	V_L	8.4	9.6	10.5	V	I_F=220mA	 	Power Consumption	P_{BL}	1.848	2.112	2.31	W	Note 1	 	LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3	 Note 1: The LED driving condition is defined for LED module (33LED). The voltage range will be 8.4V to 10.5V based on suggested driving current set as 220mA.
		18	Brightness: min 400nits Udate RGB Chromaticity.
1.1	2011/03/11	8	Add: Operating Temp. -20~70 ; Storage Temp. -30~80 ^{0}C
		10	Updade VCOM =2.27
		21 & 22	Image Sticking: 25^{0}C, Add Storage & Operation range reference chart
1.2	2011/03/24	8	Add: Absolute Operating Temp. -20~70 ; Storage Temp. -30~80 ^{0}C
1.3	2012/11/30	24	Modify packing form and increase packing quantity per carton
1.4	2013/9/26	9	Update Electric DC Characteristics Table
		11	Update Timing Table
		12	Add note 3 of input timing setting
		15	Add R43 setting description
		16	Update Power On and Off Sequence
1.5	2017/01/03	8	Modify Backlight Pin Assignment table

Contents

A. General Information

This product is for car after-market. digital photo frame and other suitable application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	7(Diagonal)	
2	Display Resolution	dot	800(H)×480RGB(V)	
3	Overall Dimension	mm	165(H) × 104(V) × 5.1(T)	Note 1
4	Active Area	mm	152.40(H)×91.44(V)	
5	Pixel Pitch	mm	0.1905(H)×0.1905(V)	
6	Color Configuration	--	Tri-Gate	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	160	
12	Panel Power Consumption	mW	0.19	Note 4
13	Backlight Power Consumption	W	2.112 (typ)	
	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.
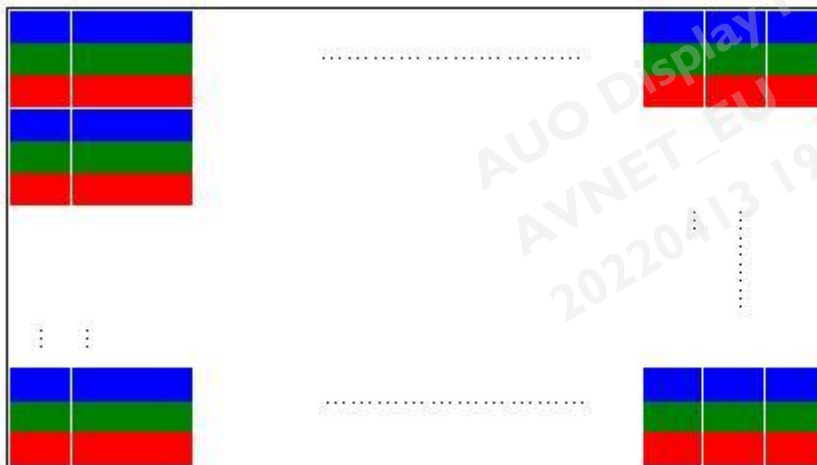
(1 2 3..............................798 799 800)

Note 3: The full color display depends on 24-bit data signal **(pin 33~40, 42~49, 51~58)**

Note 4: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module – Front View

NOTES:
1.GENERAL TOLERANCE: ± 0.3 mm.
2.THE BENDING RADIUS OF FPC SHOULD BE
   LARGER THAN 0.6 mm.
3.CONNECTOR: E&T H20IK-P02N-02B

165±0.3 (OUTLINE)
154.4±0.3 (BEZEL OPENING)
(152.4)(ACTIVE AREA)
(80.2)
5.1±0.3 (WITHOUT LABEL)

2.78
(3.78)
(49.5)

DISPLAY CENTER

104±0.3 (OUTLINE)
93.44±0.3 (BEZEL OPENING)
(91.44) (ACTIVE AREA)

W=0.35±0.03
3.5±0.3

60

2-0.5±0.1
P0.5*(60-1)=29.5±0.05
30.5±0.05

DETAIL A
SCALE 2/1

FPC BENDING AREA

60±5

PIN I (+)
COLOR: WHITE

PIN2 (-)
COLOR: BLACK

(4.87)
45.29±1

COMPONENT HEIGHT: 1.2mm (MAX.)

(14.33)

64.86±1

80.11±1

60   1

SEE DETAIL A

0.3±0.05
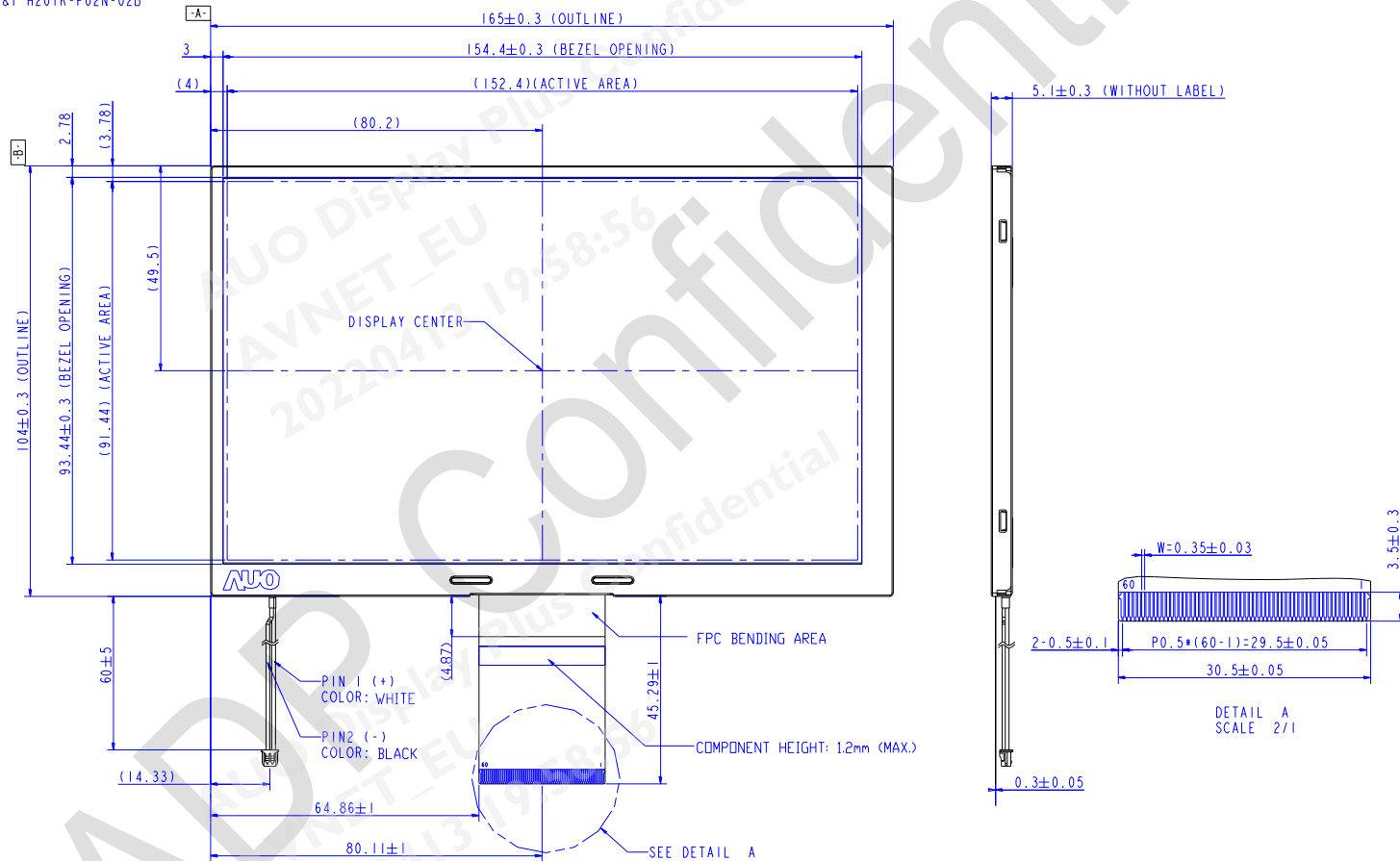
2. TFT-LCD Module – Rear View

(31)   (67)   -A-

-B-

(16.4)

(13)

MODULE LABEL

(84.6)

(13)

BLU LABEL

(31)   (6.4)
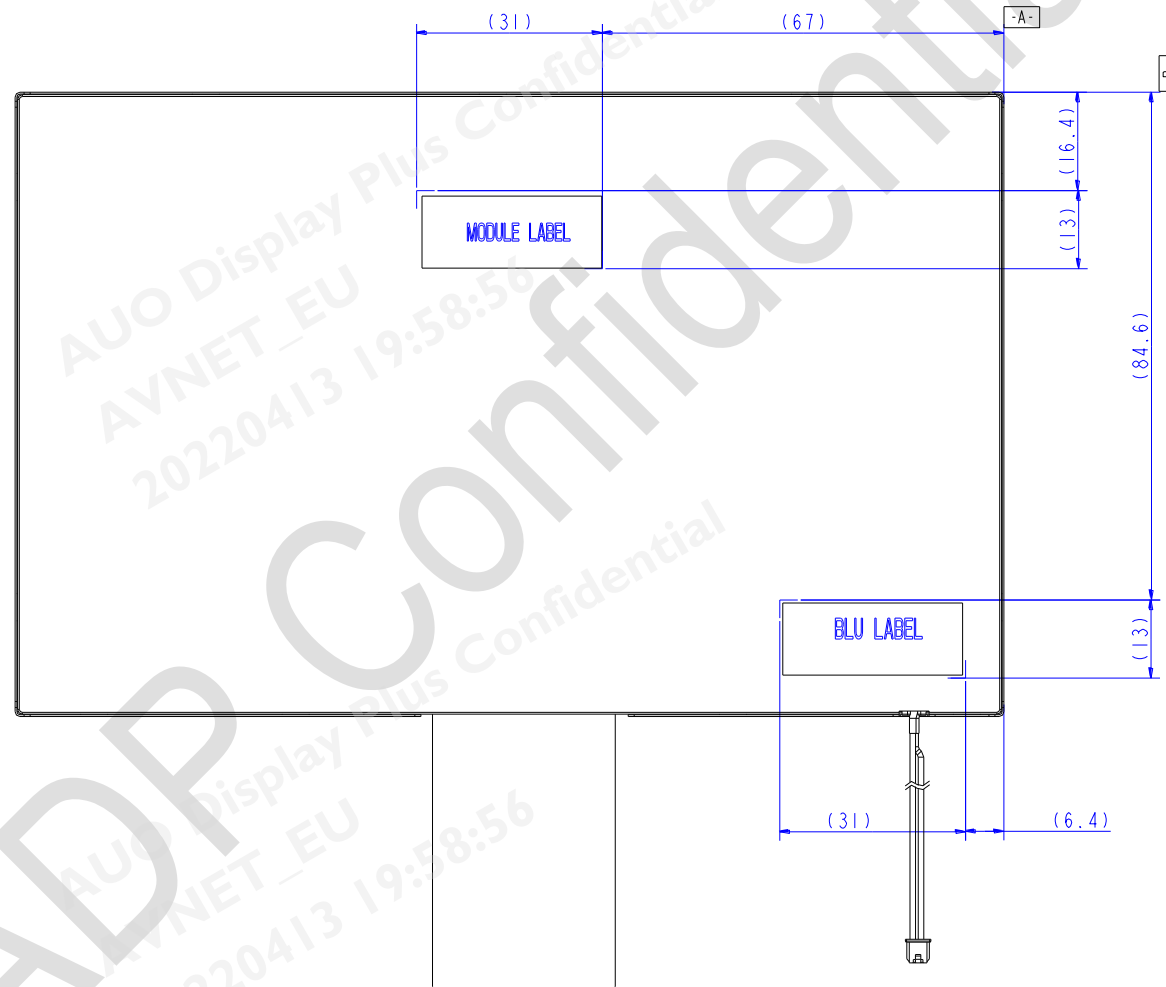
C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Recommended connector :

Pin No.	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving voltage	
2	VGL	P	Negative power supply voltage for Gate driver	
3	VGH	P	Positive power supply voltage for Gate driver	
4	VGH	P	Positive power supply voltage for Gate driver	
5	VDPA	P	Positive Supply voltage for analog power	
6	VDNA	P	Negative Supply voltage for analog power	
7	GND	P	Ground for digital circuit	
8	DRV_BLU	O	OUTPUT_PWM_SIGNAL output via an output buffer	
9	CABC_EN	I	CABC function enable (**active high**)	
10	UD	P	Up / Down Select	Note2
11	RL	O	Right / Left Select	Note2
12	GRB	I	Global reset pin (**active low: reset when GRB='L'**)	Note1
13	V10	I	Gamma correction voltage reference	
14	V9	I	Gamma correction voltage reference	
15	V8	I	Gamma correction voltage reference	
16	V7	I	Gamma correction voltage reference	
17	V6	I	Gamma correction voltage reference	
18	V5	I	Gamma correction voltage reference	
19	V4	I	Gamma correction voltage reference	
20	V3	I	Gamma correction voltage reference	
21	V2	I	Gamma correction voltage reference	
22	V1	I	Gamma correction voltage reference	
23	VDDIO	P	Supply voltage for digital circuit	
24	VDDIO	P	Supply voltage for digital circuit	
25	CS	I	Chip select (Low active) of SPI	
26	SDA	I/O	Data input/output of SPI	
27	SCL	I	Clock input of SPI	
28	GND	P	Ground for digital circuit	
29	DCLK	I	Data clock Input	
30	GND	P	Ground for digital circuit	
31	DE	I	Data enable Input	
32	GND	P	Ground for digital circuit	

33	DB7	I	Blue data input **(MSB)**	
34	DB6	I	Blue data input	
35	DB5	I	Blue data input	
36	DB4	I	Blue data input	
37	DB3	I	Blue data input	
38	DB2	I	Blue data input	
39	DB1	I	Blue data input	
40	DB0	I	Blue data input **(LSB)**	
41	GND	P	Ground for digital circuit	
42	DG7	I	Green data input **(MSB)**	
43	DG6	I	Green data input	
44	DG5	I	Green data input	
45	DG4	I	Green data input	
46	DG3	I	Green data input	
47	DG2	I	Green data input	
48	DG1	I	Green data input	
49	DG0	I	Green data input **(LSB)**	
50	GND	P	Ground for digital circuit	
51	DR7	I	Red data input **(MSB)**	
52	DR6	I	Red data input	
53	DR5	I	Red data input	
54	DR4	I	Red data input	
55	DR3	I	Red data input	
56	DR2	I	Red data input	
57	DR1	I	Red data input	
58	DR0	I	Red data input **(LSB)**	
59	GND	P	Ground for digital circuit	
60	VCOM	I	Common electrode driving voltage	

I: Input; P: Power

Note1: Global reset, normally pulled high. Suggest to connecting with an RC (R=10K ohm, C=1uF)
reset circuit for stability. Normally pull high.

Note2:

U/D	Direction	**L/R**	Direction
H	D → U	H	R → L
L	U → D	L	L → R

TOP

LEFT

RIGHT

ACTIVE AREA CENTER

BOTTOM
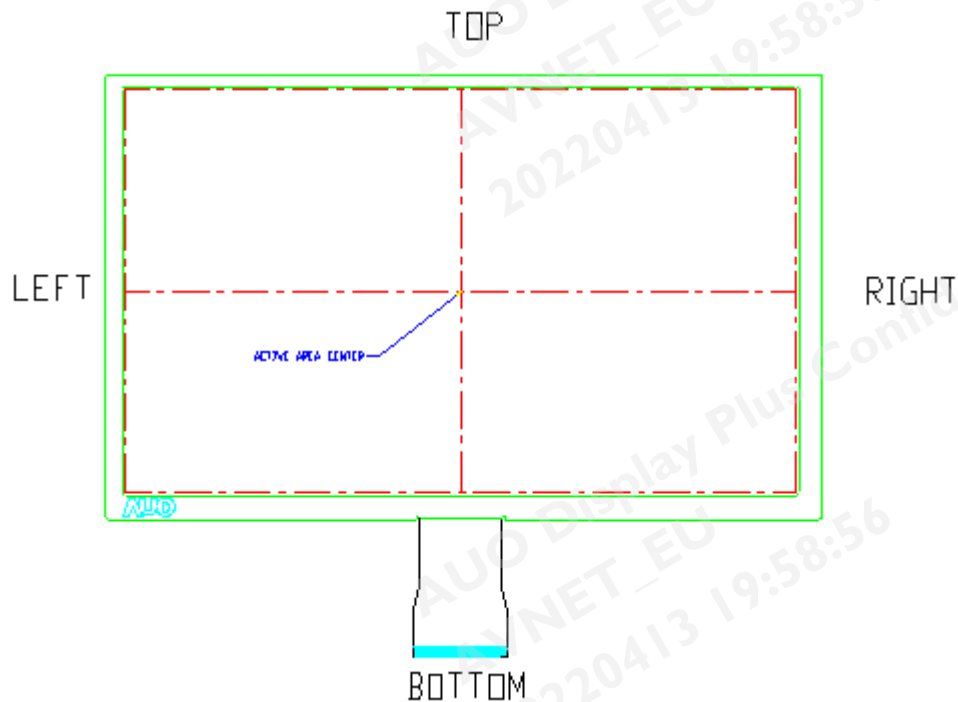
2. Backlight Pin Assignment

Recommended connector : E&T H201K-P020N-02B

Color	Symbol	I/O	Description	Remark
RED	VLED	P	LED anode	
BLACK	VLED	P	LED cathode	

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDDIO	GND=0	-0.5	5	V	
	VDPA	GND=0	-0.5	5.9	V	
	VDNA	GND=0	-5.9	0.5	V	
	VGH - VGL	GND=0	-	32	V	
Input signal voltage	Vi	GND=0	-0.3	VDDIO+0.3	V	Note 1
	VCOM	GND=0	-3.5	0		
	V1~V5	GND=0	0	VDPA-0.2		
	V6~V10	GND=0	VDNA+0.2	0		
Operating Temperature	Topa		-20	70	℃	
Storage temperature	Tstg		-30	80	℃	

Note 1:De, Digital Data

Note 2:Functional operation should be restricted under ambient temperature (25℃).

Note 3:Maximum ratings are those values beyond which damages to the device may occur. Functional

operation should be restricted to the limits in the Electrical Characteristics chapter.

4. Electrical DC Characteristics

a. (VCC = +3.3V, VDPA=5V, VDNA=-5V, AGND=GND=0V, TOPR = -10°C to +60°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		VCC	3.0	3.3	3.6	V	Digital power
		VDPA	4.5	5	5.5	V	Analog Power
		VDNA	-5.5	-5	-4.5	V	Analog Power
		VGH	13.3	14	14.7	V	Positive power supply for gate driver
		VGL	-14.7	-14	-13.3	V	Negative power supply for gate driver
Input Signal Voltage	H Level	VIH	VDDIOx0.7	-	VDDIO	V	Note 1
	L Level	VIL	GND	-	0.3xVDDIO	V	
Gamma reference voltage		VCOM1	-2.77	-2.27	-1.77	V	UD = "L", Note 3.
		VCOM2	-3.17	-2.67	-2.17	V	UD = "H", Note 3
		V1		4.21		V	Detail Gamma voltage please refer to page 26 Note 2
		V2		2.84			
		V3		2.36			
		V4		1.96			
		V5		0.98			
		V6		-1			
		V7		-2.01			
		V8		-2.42			
		V9		-2.92			
		V10		-4.33			

Note 1: DE , Digigal Data

Note 2: VDPA > V1 > V2 > V3 > V4 > V5 > V6 > V7 > V8 > V9 > V10 > VDNA

Note 3: VCOM1 when UD ="L", display from up to down.
VCOM2 when UD ="H", display from down to up.

b. Current Consumption (AGND=GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VCC	I$_{VDD}$	VCC=3.3V	-	6.23	9	mA	Note 1
Inpur current for VDPA	I$_{VDPA}$	VDPA=5V	-	5.42	12.9	mA	Note 1
Input current for VDNA	I$_{VDNA}$	VDNA=-5V	-	-5.44	-13.4	mA	Note 1
Inpur current for VGH	I$_{VGH}$	VGH=14V	-	3.88	5	mA	Note 1
Inpur current for VGL	I$_{VGL}$	VGL= -14V		-3.94	-5	mA	Note 1
Inpur current for VCOM	I$_{VCOM}$	VCOM=2.27V		6.23	9	mA	Note 1

Note 1: The test pattern use the following pattern.

c. Backlight Driving Conditions

The backlight (LED module, Note 1) is suggested to drive by constant current 220mA.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED light bar Voltage	V$_L$	8.4	9.6	10.5	V	I$_F$=220mA
Power Consumption	P$_{BL}$	1.848	2.112	2.31	W	Note 1
LED Life Time	L$_L$	10,000	--	--	Hr	Note 2, 3

Note 1: The LED driving condition is defined for LED module (33LED). The voltage range will be 8.4V

to 10.5V based on suggested driving current set as 220mA.
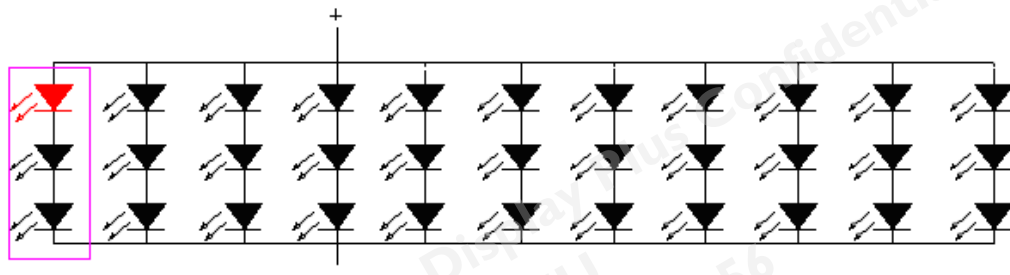
Note 2: Define "LED Lifetime": brightness is decreased to 50% of the initial value. LED Lifetime is

restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 220mA.

Note 3: If it uses larger LED lightbar voltage/ current more than 10.5V/220mA, it maybe decreases the

LED lifetime.

5. Electrical AC Characteristics

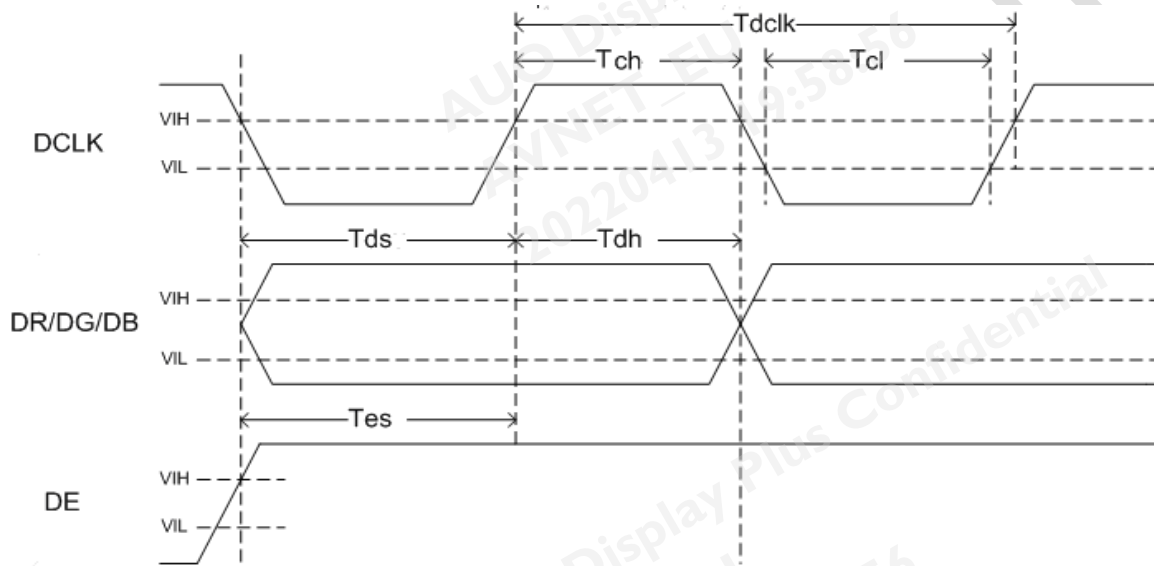### a. Signal AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock High time	Tch		8	-	-	ns
Clock Low time	Tcl		8	-	-	ns
Data setup time	Tds		5			ns
Data hold time	Tdh		10			ns
Data enable set-up time	Tes		4			ns

b. Input timing Setting (DE Mode only)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remark
DCLK frequency	F$_{DCLK}$	30.3	33.26	37.8	MHz	
Hsync period (= Thd + Thbl)	Th	1000	1056	1112	T$_{DCLK}$	Note 1,2
Active Area	Thd	--	800	--	T$_{DCLK}$	
Horizontal blanking (= Thf+ The)	Thbl	200	256	312	T$_{DCLK}$	
Vsync period (= Tvd + Tvbl)	Tv	517	525	532	Th	
Active lines	Tvd	--	480	--	Th	
Vertical blanking (=Tvf + Tve)	Tvbl	37	45	52	Th	

Vertical timing:
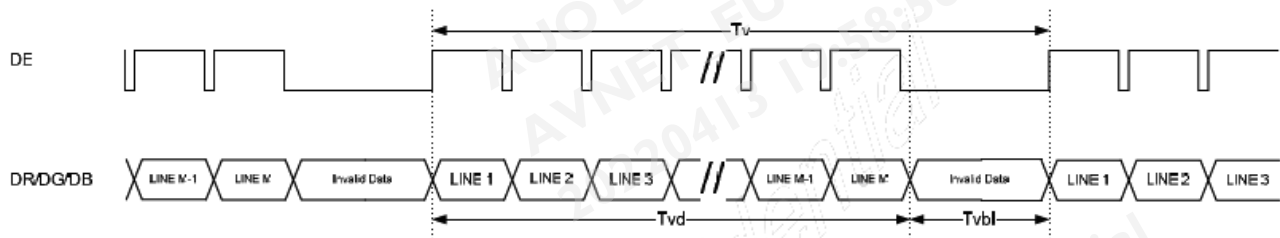
Horizontal timing:
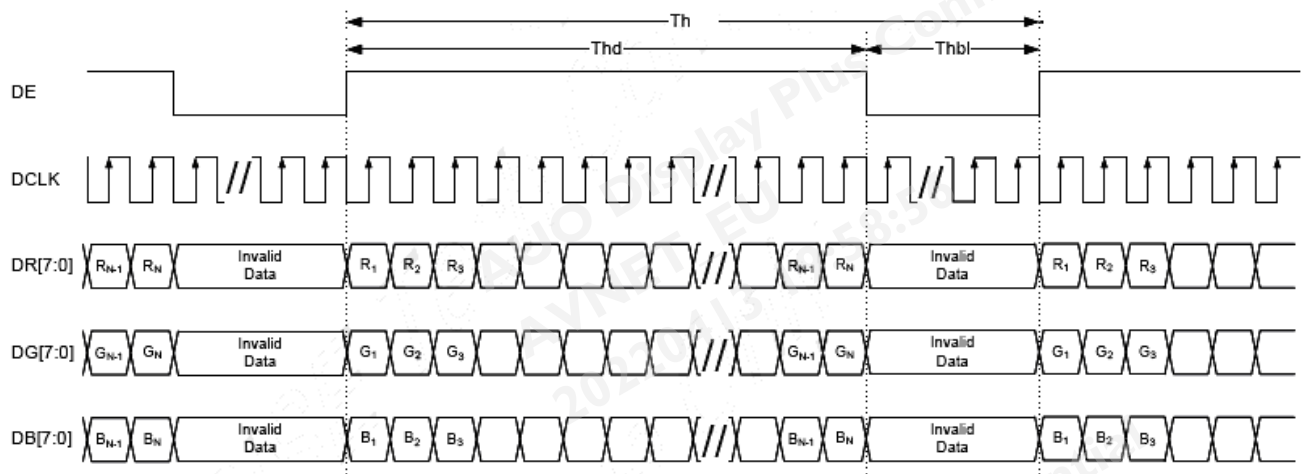
Note: horizontal resolution N = 800

Note: vertical resolution M = 480

Note 1: If input timing operates with Min. to Typ. setting, the PWCK value use default value 1973 (Register R39=0000_0111, Register R40=1011_0101), and no need to change SPI register.

Note 2: If input timing operates with Typ. to Max. setting, the PWCK value must be set to 2025(Register R39=0000_0111, Register R40=1110_1001). Please reference the Serial interface setting table in Page.16 to set SPI Register R39 and R40 value.

Note 3 :Input timing setting should be kept the same and lcd data clock cann't interrupt after power on sequence.

6. Serial Interface Characteristics

a.Serial Control Interface AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial clock	Tsck	320			ns	
SCL pulse duty	Tscw	40%	50%	60%	Tsck	
Serial data setup time	Tist	120			ns	
Serial data hold time	Tihd	120			ns	
Serial clock high/low	Tssw	120			ns	
CS setup time	Tcst	120			ns	
CS hold time	Tchd	120			ns	
Chip select distinguish	Tcd	1			us	
Delay from CSB to Vsync	Tcv	1			us	

AC serial interface write mode timings
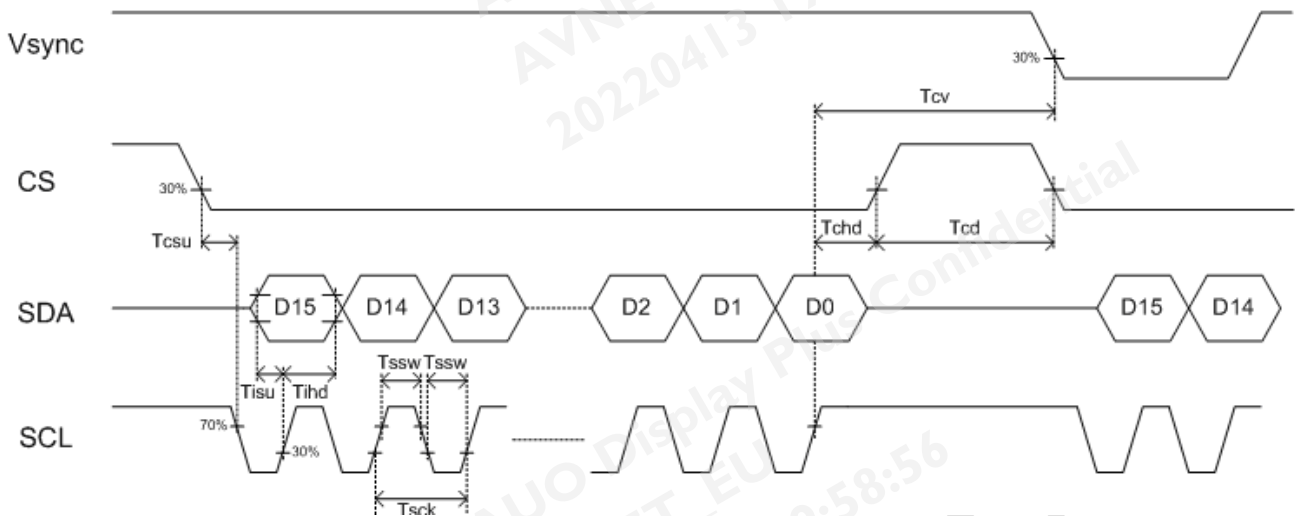
b. Register Bank

A totally 16-bit register including 7-bit address D[15:9], 1-bit R/W bit D[8] and 8-bit data D[7:0] can be set via 3-wire serial peripheral interface. Below figure is for a detail description of the parameters.
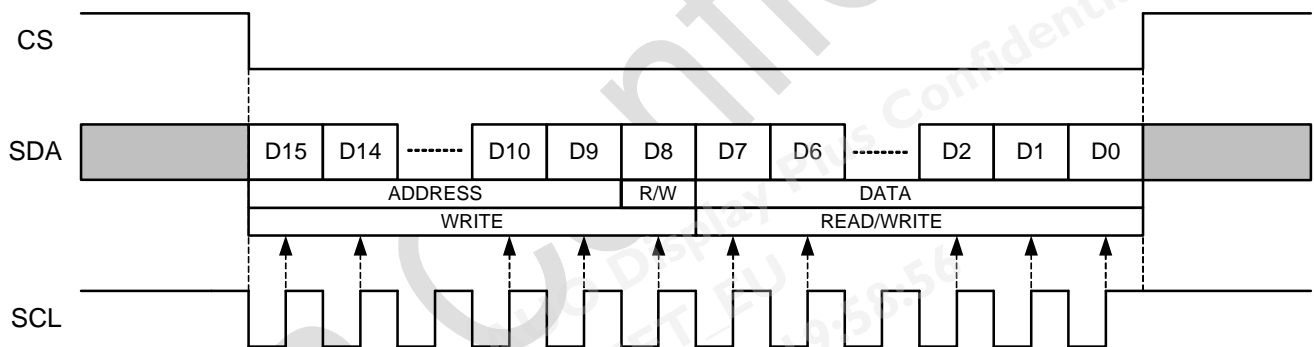
Figure: Serial interface write/read sequence

◆ Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

◆ Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

◆ The serial control block is operational after power on reset, but commands are established by the following the following rising edge of the End Frame(DE mode). If command is transferred multiple times for the same register, the last command before the following rising edge of the End Frame(DE mode) is valid, except for some special registers (ex. GRB, etc.).

◆ If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

  - The write operation is cancelled.

  - The read operation is interrupt.

◆ If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data in the duration of CS="L" are valid data.

◆ Serial block operates with the SCL clock.

◆ Serial data can be accepted in the standby (power save) mode.

◆ Register R/W setting: D8 = "L" → write mode; D8 = "H" → read mode.

◆ It is suggested that DE,DCLK(for DE mode) always exists in the same time.

c.Serial Interface Setting Table.

Reg	ADDRESS							R	DATA							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	--	--	--	1 note 1	1 note 1	1 note 1	0	1
R1	0	0	0	0	0	0	1	0	0 note 1	0 note 1	--	--	00		00	
R39	0	1	0	0	1	1	1	0	--	--	--	--	PW_CK			
R40	0	1	0	1	0	0	0	0	PW_CK							

Note 1: The value of this bit could not be change. Otherwise the Panel will display abnormal.

d.Register Description

R0 settings

Address	Bit		Discription	Default
000000	7 - 2	--	AUO internal use	000111
	1	STB	Standby mode setting	0
	0	GRB	S/W global reset	1

Bit 1	STB
0	Nomal operation **(default)**
1	Standby mode. Register data are kept.

Bit 0	GRB
0	S/W global reset. Reset all register to default value. H/W GRB has higher priority.
1	Normal operation. **(default)**

S/W GRB	H/W GRB	Operation mode
0	0	H/W reset
0	1	Execute S/W reset procedure
1	0	H/W reset
1	1	Normal operation

R1 Settings

Address	Bit		Discription	Default
000001	7 - 4	--	AUO internal use	0000
	3 - 2	CHUD	Vertical scan direction setting	00
	1 - 0	CHLR	Horizontal scan direction setting	00

Bit 3 - 2	CHUD	
0x	Accoring to H/W pin U/D setting. **(default)**	
10	Vertical scan direction is from up to down.	
11	Vertical scan direction is from down to up.	

Bit 1 - 0	CHLR	
0x	Accoring to H/W pin L/R setting. **(default)**	
10	Horizontal scan direction is from left to right.	
11	Horizontal scan direction is from right to left.	

R39 setting

Address	Bit		Discription	Default
100111	3 - 0	--	AUO PW_CK default value	0111
	3 - 0	--	AUO PW_CK Max value	0111

R40 setting

Address	Bit		Discription	Default
101000	7 - 0	--	AUO PW_CK default value	1011_0101
	7 - 0	--	AUO PW_CK Max value	1110_1001

R43 setting

Address	Bit		Discription	Default
101011	7 - 0	--	AUO BI_Delay default value	0101_0101
	7 - 0	--	AUO BI_Delay suggestion value	0100_0011

Note : BI_Delay must be set as the suggestion value for better stabilization of LCD

7. Power On/Off Characteristics

This IC may be damaged by a large current flow when an incorrect power sequence is applied. The recommended power-on sequence is to first connect the logical power (VDDIO&GND), then the global reset including GRB reset or SPI command(R0), and then the digital signal (DCLK,DE). After DCLK and DE are active, VDPA,VDPA VGL and VGH need be ready and register R39、R40 and R43 should be set correctly within 80 ms. Finally, following the power on sequence, panel can normally start up.

a. Recommended Power On and Off Sequence

Note 1: If input timing operates with Min. to Typ. setting, the PWCK value use default value 1973 (Register R39=0000_0111, Register R40=1011_0101), and no need to change SPI register.
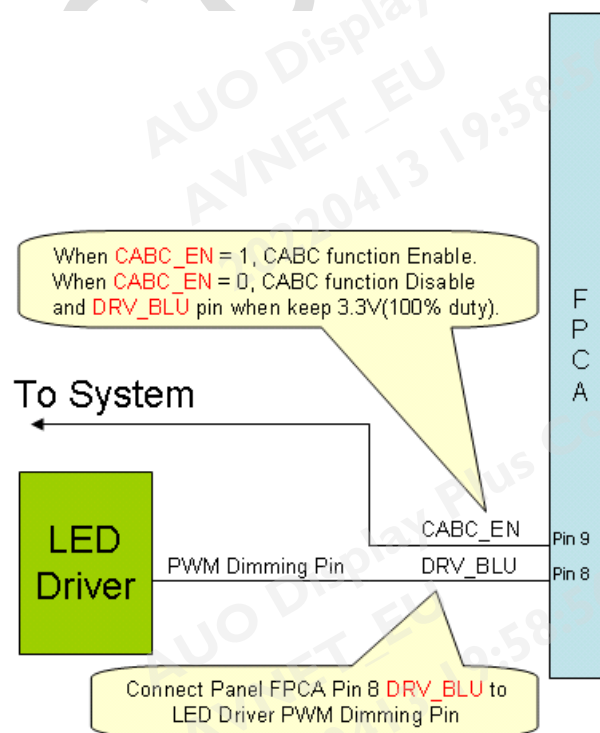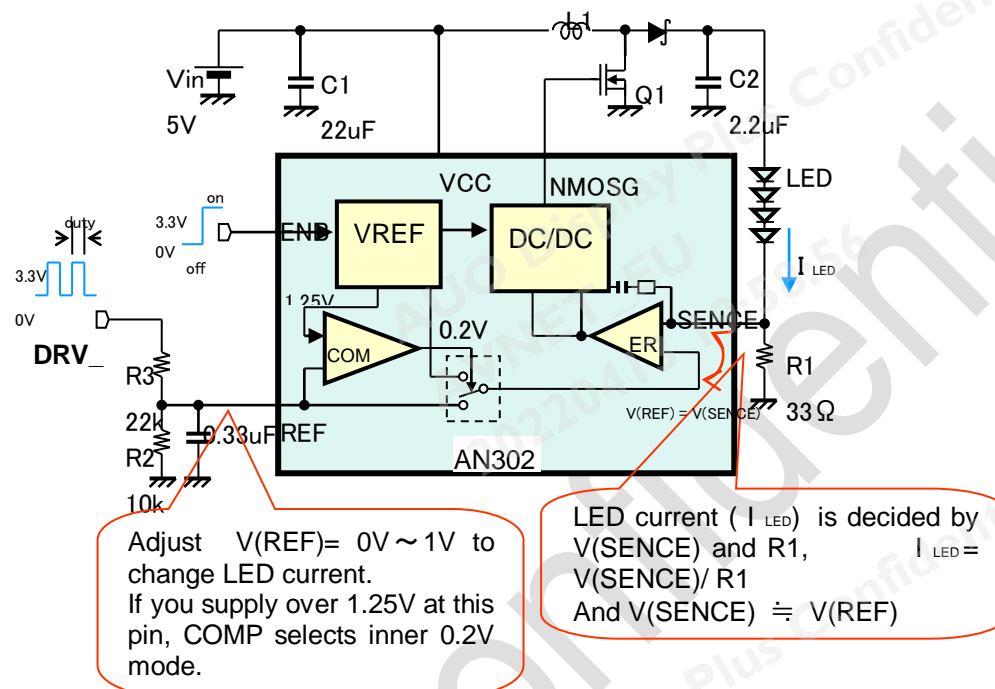
Note 2: If input timing operates with Typ. to Max. setting, the PWCK value must be set to 2025(Register R39=0000_0111, Register R40=1110_1001). Please reference the Serial interface setting table in Page.15 to set SPI Register R39 and R40 alue.
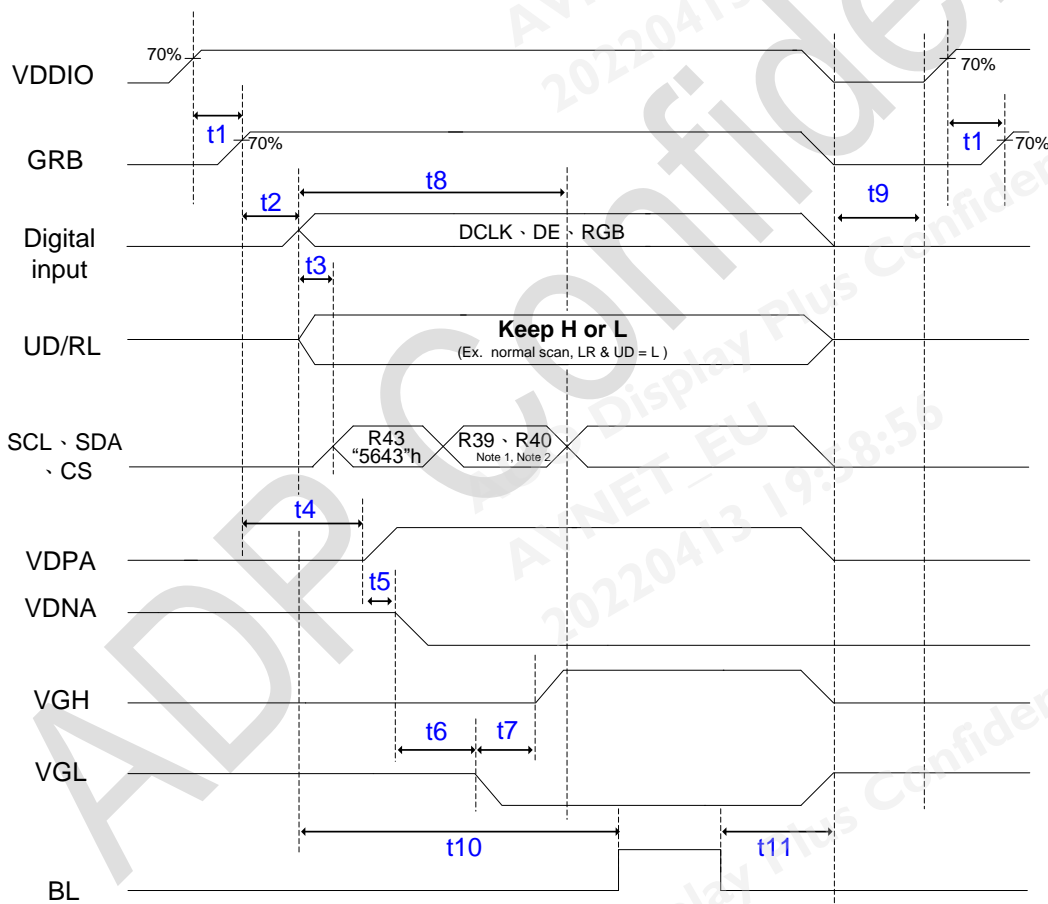
t1 >= 10us, t2 >= 30ms, 50ms >= t3 >= 40ms, t4 >= 0ms, t5 >= 0ms, t6 >= 0ms, t7 >= 0ms, 80ms >= t8, t9 >= 1s, t10 >= 200ms, t11 >= 20ms

8. Content-based Automatic Backlight Control (CABC) reference circuit

It is used in a step-up DCDC converter that drives an external NMOS power transistor using a constant frequency PWM architecture. With 2 current modes (Dimmi Mode / Normal Mode) selectable.

Adjust V(REF)= 0V ～ 1V to change LED current.
If you supply over 1.25V at this pin, COMP selects inner 0.2V mode.

LED current (I_{LED}) is decided by V(SENCE) and R1, $I_{LED} =$ V(SENCE)/ R1
And V(SENCE) ≒ V(REF)

When CABC_EN = 1, CABC function Enable.
When CABC_EN = 0, CABC function Disable and DRV_BLU pin when keep 3.3V(100% duty).

To System

LED Driver

PWM Dimming Pin

CABC_EN   Pin 9
DRV_BLU   Pin 8

FPCA

Connect Panel FPCA Pin 8 DRV_BLU to LED Driver PWM Dimming Pin

D.   Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time								
	Rise	Tr	θ=0°	--	12	20	ms	Note 3
	Fall	Tf		--	18	30	ms	
Contrast ratio		CR	At optimized viewing angle		500	--		Note 4
Viewing Angle	Top		CR≧10	40	50		deg.	Note 5
	Bottom			50	60			
	Left			55	65			
	Right			55	65			
Brightness		Y_L	θ=0°	400	500	--	cd/m²	Note 6
Chromaticity	White	X	θ=0°	0.26	0.31	0.36		
		Y	θ=0°	0.28	0.33	0.38		
	Red	X	θ=0°	0.56	0.61	0.66		
		Y	θ=0°	0.30	0.35	0.40		
	Green	X	θ=0°	0.29	0.34	0.39		
		Y	θ=0°	0.51	0.56	0.61		
	Blue	X	θ=0°	0.11	0.16	0.21		
		Y	θ=0°	0.07	0.12	0.17		
Uniformity		$\triangle Y_L$	%	70	75	--	%	Note 7

Note 1: Ambient temperature =25℃, and LED lightbar current::220mA. To be measured in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter

BM-5A, after 15 minutes operation.
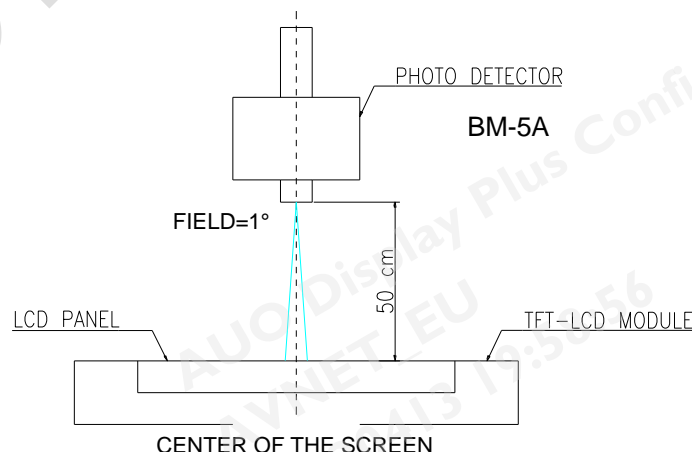
Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.
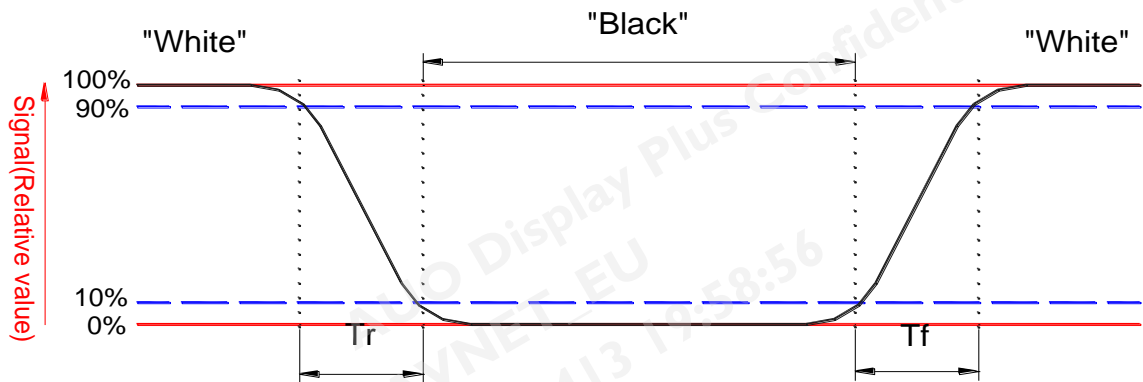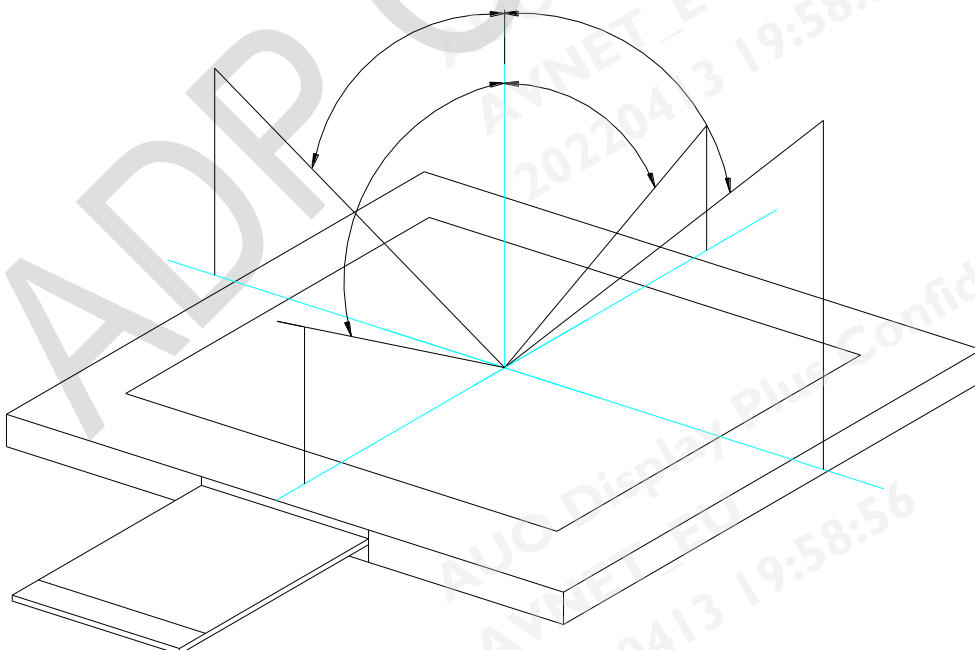

Note 4．Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at " White" status}}{\text{Photo detector output when LCD is at " Black" status}}$$

Note 5. Definition of viewing angle, θ , Refer to figure as below.

Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically
opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:
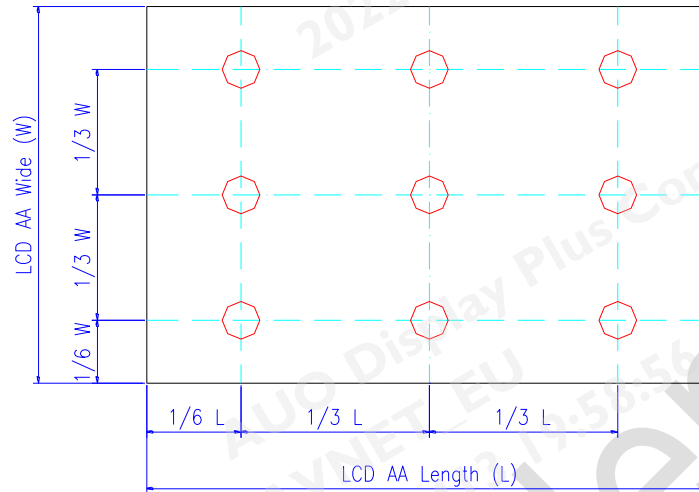
$$Uniformity = \frac{minimum\ luminance\ in\ 9\ points\ (1-9)}{maximum\ luminance\ in\ 9\ points\ (1-9)}$$

E. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 80℃	240Hrs	Note 4
2	Low Temperature Storage	Ta= -30℃	240Hrs	
3	High Ttemperature Operation	Tp= 70℃	240Hrs	
4	Low Temperature Operation	Ta= -20℃	240Hrs	
5	High Temperature & High Humidity	Tp= 50℃. 80% RH	240Hrs	Operation
6	Heat Shock	-20℃~70℃, 50 cycle,	2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B		Note 5
8	Image Sticking	25℃, 4hrs		Note 6
9	Vibration	Frequency range : 10Hz~55Hz Stoke : 1.5mm Sweep : 10Hz~55Hz~10Hz 2 hours for each direction of X,Y,Z. Total 6 hours.		Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction		Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		
13	Pressure	5kg, 5sec		Note 7

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

Note4 : Storage & Operation range reference chart.
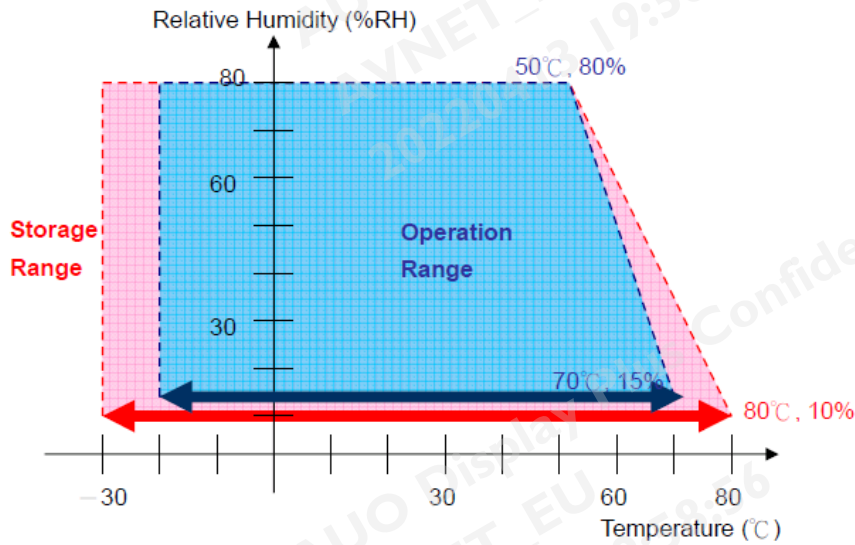
Note5 : All test techniques follow IEC6100-4-2 standard.

Test Condition		Note
Pattern		
Procedure And Set-up	<u>Contact Discharge</u>：330Ω, 150pF, 1sec, 8 point, 25times/point <u>Air Discharge</u>：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 6: Operate with chess board pattern as figure and lasting time and temperature as the conditions.

Then judge with 50% gray level, the mura is less than JND 2.5
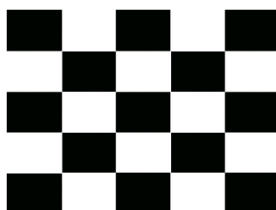
Note 7: The panel is tested as figure. The jig is ϕ 10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)
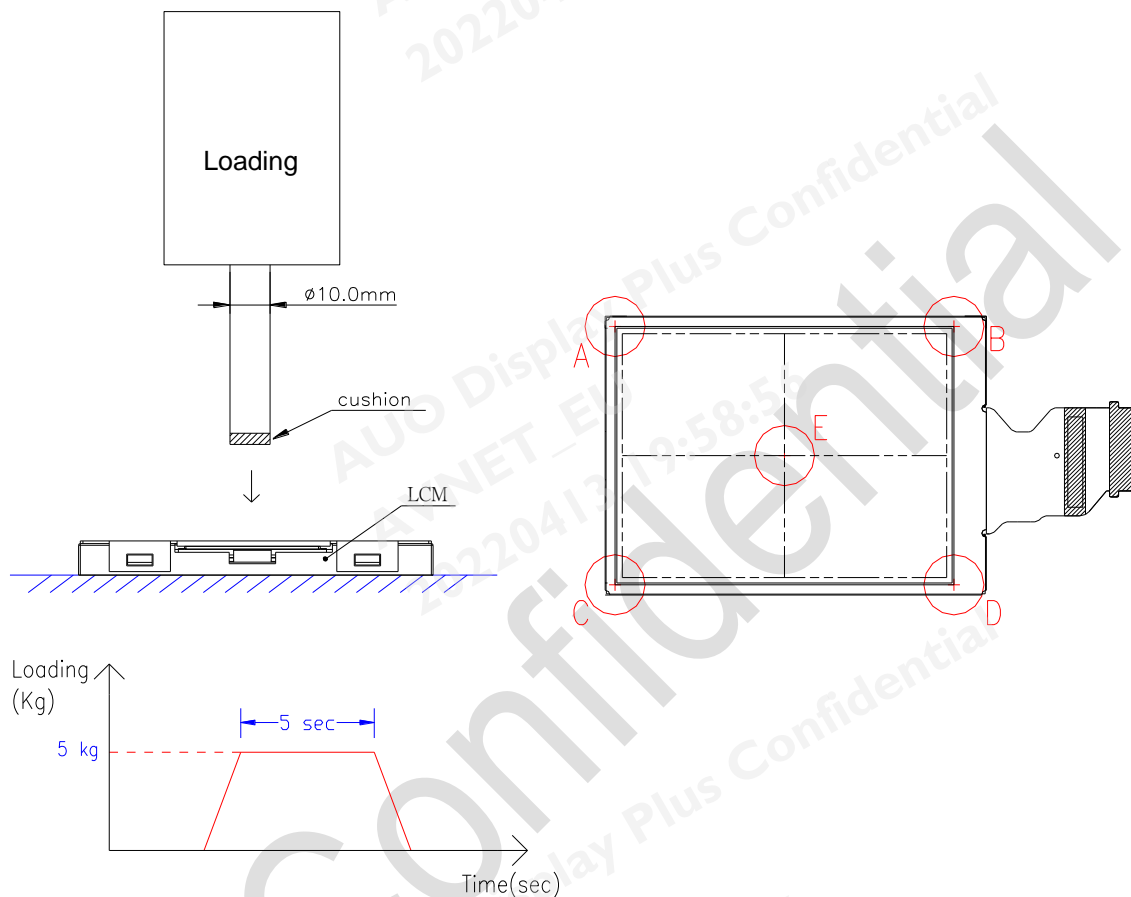
F. Packing and Marking

1. Packing Form
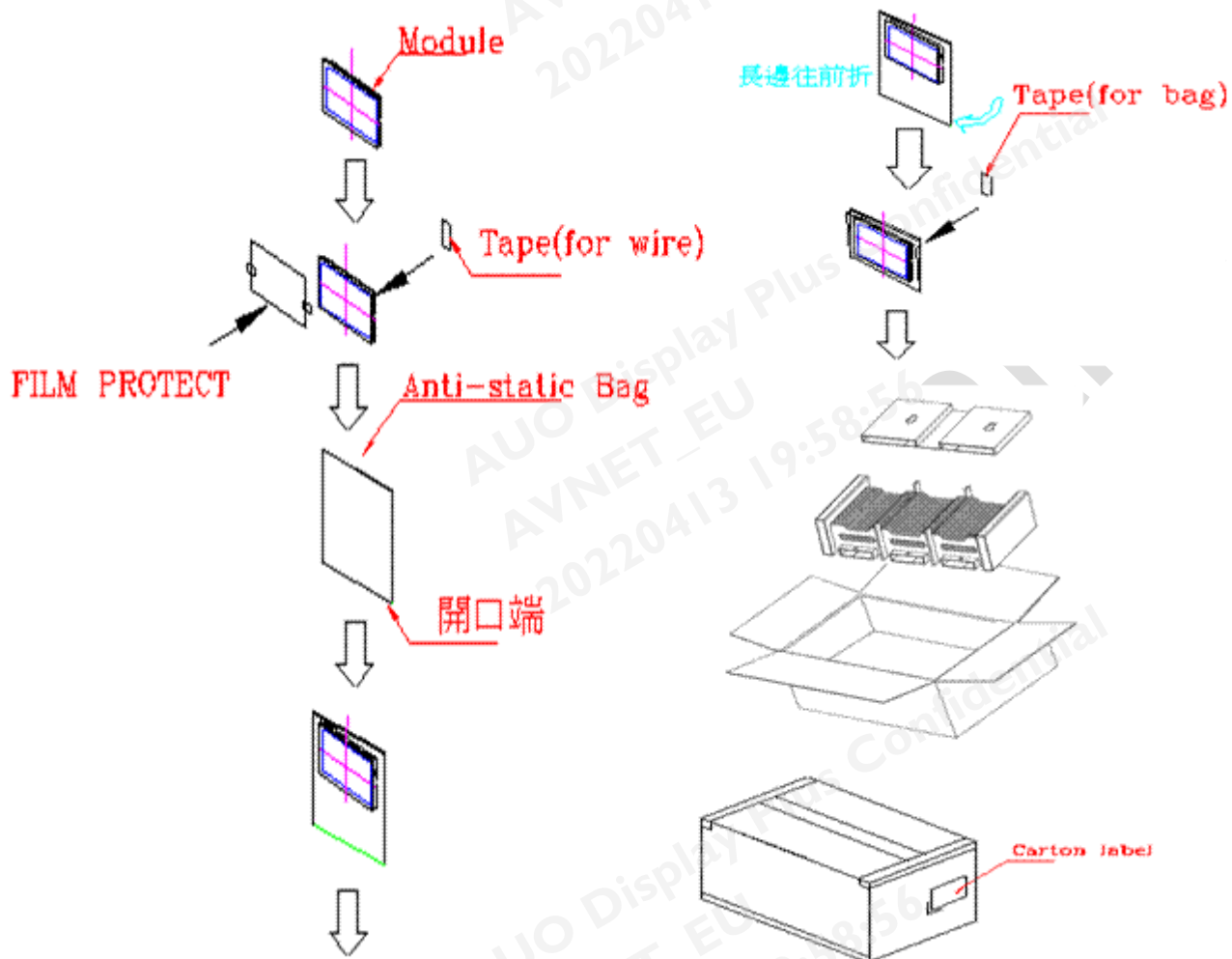
Max capacity: 60 TFT-LCD module per carton
Max weight: 12.0 kg per carton
Outside dimension of carton: 600mm(L)*353mm(W)*210mm(H)
Pallet size: 1230 mm * 1110 mm * 135 mm

2. Module/Panel Label Information

The module/panel (collectively called as the "Product") will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:

ABCDEFGHIJKLMNOPQRSTUV

— For internal system usage and production serial numbers.

— AUO Module or Panel factory code, represents the final production factory to complete the Product

— Product version code, ranging from 0~9 or A~Z (for Version after 9)

— Week Code, the production week when the product is finished at its production process

3. Carton Label Information

The packing carton will be attached with a carton label where packing Q'ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:

ABC-DEFG-HIJK-LMN

— DEFG appear after first "-" represents the packing date of the carton

— Date from 01 to 31

— Month, ranging from 1~9, A~C. A for Oct, B for Nov and C for Dec.

— A.D. year, ranging from 1~9 and 0. The single digit code reprents the last number of the year

Refer to the drawing of packing format for the location and size of the carton label.

G. Reference application circuit

1. Recomonded Gamma Voltage

Symbol	Value (V)
V1	4.21
V2	2.84
V3	2.36
V4	1.96
V5	0.98
V6	-1
V7	-2.01
V8	-2.42
V9	-2.92
V10	-4.33
VDPA	+5
VDNA	-5

2. Application Circuit

VDPA_DCDC : 5V

FBP:1.213V

R32 = R33 * (VDPA/VREF -1)

VREF : 1.213V

FBN: 0V

R39 = R38 * (- VNGE/VREF)

VDNA_DCDC : -5V

VGH_DCDC : 14V

8.9V

VGL_DCDC : -14V

VDNA_DCDC

LX_N

NC R51 0ohm
5% 0603

R49 0ohm 5% 0603

VDNA_N1X PAD

C27 100nF X7R
25V 0603 0.81~0.90mm

D10 BAV99TGP

N1X

NC R95 0ohm 5% 0603

C31 2.2uF X7R 25V 1.41~1.60mm 0805

VDNA_N2X PAD

C35 100nF X7R
25V 0603 0.81~0.90mm

D12 BAV99TGP

N2X

R57 0ohm 5% 0603

C37 2.2uF X7R 25V 1.41~1.60mm 0805

VDNA_N3X PAD

C38 100nF X7R
25V 0603 0.81~0.90mm NC

D13 BAV99TGP NC

N3X

R61 15.0Kohm 5% 0603 NC

VGLA PAD

VGLA

R62 0ohm 5% 0603

VGL_DCDC

C40 2.2uF X7R 25V 1.41~1.60mm 0805 NC

NC D14 MMPZ5244BGP

C41 2.2uF X7R 25V 1.41~1.60mm 0805

R64 47.0Kohm 5% 0603

VCOM_OP1 PAD

R67 0ohm 5% 0603

VCOM

VCOM

U4
5 V+ Vout
4 Vin- V-
Vin+
G1562TO1

VDNA_DCDC

C42 10uF X7R 16V 1.81~2.00mm 1206

C43 100nF X7R 25V 0.81~0.90mm 0603

VCOMIN1 PAD

R93 0ohm 5% 0603

VCOM_T

C44 10uF X7R 16V 1.81~2.00mm 1206

R92 10Kohm 25% VCOMIn

C49 10uF X7R 16V 1.81~2.00mm 1206

R94 1.30Kohm

VDNA_DCDC

H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.

2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.

3. Avoid dust or oil mist during assembly.

4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.

5. Less EMI: it will be more safety and less noise.

6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.

7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.

8. Be sure to turn off the power when connecting or disconnecting the circuit.

9. Polarizer scratches easily, please handle it carefully.

10. Display surface never likes dirt or stains.

11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.

12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.

13. High temperature and humidity may degrade performance.   Please do not expose the module to the direct sunlight and so on.

14. Acetic acid or chlorine compounds are not friends with TFT display module.

15. Static electricity will damage the module, please do not touch the module without any grounded device.

16. Do not disassemble and reassemble the module by self.

17. Be careful do not touch the rear side directly.

18. No strong vibration or shock. It will cause module broken.

19. Storage the modules in suitable environment with regular packing.

20. Be careful of injury from a broken display module.

21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.