

SPECIFICATION

PRODUCT NO.: TCXD088ABLGA-1

VERSION : Ver 1.3 **ISSUED DATE** : 2022-11-09

This module uses ROHS2.0 material



- O: APPROVAL FOR SPECIFICATION
- **■**: APPROVAL FOR SAMPLE

DATE APPROVED BY

Xinli Optoelectronics:

Presented by	Reviewed by	Organized by
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1. Revision Recode

Revision	Description	Date
1.0	Initial Release	2022/8/11
1.1	Modify power on / off timing and LVDS Signal Timing	2022/8/17
1.2	Modify power on / off timing	2022/8/22
1.3	FPC changed Gold finger face synchronously modified shape	2022/11/09
Y		



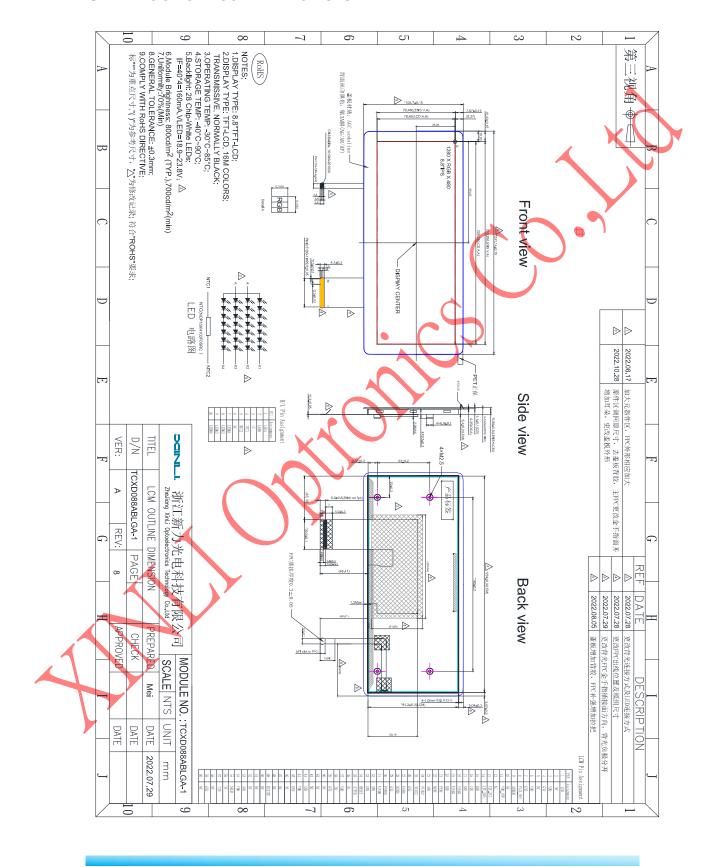
2. General Description and Features

The 8.8 inch Module named TCXD088ABLGA-1 is a-Si TFT-LCD module, which is the type of transmissive. It is consisted of TFT-LCD Panel, Driver IC, FPC and Back-Light unit. Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outsize	231.37*100.92*6.88	mm
(2)	LCD Active area	209.28 * 78.48	mm
(3)	Dot Number	1280*RGB*480	1
4)	Pixel size	0.1635*0.1635	mm
(5)	LCD type	TFT Transmissive	1
(6)	Display Color	16.7M	/
(7)	Viewing direction	Free(IPS type)	O'clock
(8)	Backlight Type	28-chip LEDs	1
(9)	Power Supply	3.3 (TYP)	V
(10)	Interface type	LVDS Interface	/
(11)	Module weight	300	g
(12)	NTSC	75 (TYP)	%



3. Mechanical Dimension





4. Interface Pin Connection

4.1 CN1 The LCD Module Electrical Interface Connection

Recommended Connector typ: IMSA-9634S-60Y902_60PIN_0.5mm

NC	Symbol	Level	Description
1	GND	P	Ground
2	NC	-	No Connection
3	VDD	P	Digital Power(+3.3V)
4	GND	P	Ground
5	NC	-	No Connection
6	VDD	P	Digital Power(+3.3V)
7	GND	P	Ground
8			Fail detection signal output.
	FAIL_DET	0	FAIL_DET=H, on normal condition
			FAIL_DET=L, on error condition
9		I	Enable auto reload OTP / EEPROM every 60 frames.
			When stop reload or changing register values by
	ATREN		SPI/I2C, ATREN should be kept 0.
	AIREN	X	ATREN=H: Enable auto-reload OTP/EEPROM -
			ATREN=L: Disable auto-reload OTP/EEPROM
			For XINLI use only
10	NC))	No Connection
11		P	Power input for OTP programming (8.6V). Leave this
	VDD_OTP		pin open or connect it to VCC1 when not programming
	VDD_OTE		ОТР
4	$\chi \chi$		For XINLI use only
12	NC	-	No Connection
13	I2C_SCL	I	Serial interface clock input for I2C interface
14	I2C_SDA	I/O	Serial Interface address and data input / output for I2C
	12C_SDA		interface
15	GND	P	Ground
16	VDD	P	LVDS Power(+3.3V)
17	GND	P	Ground
18	PIND3	I	Positive LVDS differential data input
19	NIND3	I	Negative LVDS differential data input



21 PINCLK I Positive LVDS differential CLK input 22 NINCLK I Negative LVDS differential CLK input 23 GND P Ground 24 PIND2 I Positive LVDS differential data input 25 NIND2 I Negative LVDS differential data input 26 GND P Ground 27 PIND1 I Positive LVDS differential data input 28 NIND1 I Negative LVDS differential data input 29 GND P Ground 30 PIND0 I Positive LVDS differential data input 31 NIND0 I Negative LVDS differential data input 32 GND P Ground 33 GND P Ground 34 RESET I GROUND 35 GND P Ground 36 GND P Ground 37 GND P Ground 38 GND P Ground 39 FIND0 I Negative LVDS differential data input 30 PIND0 I Negative LVDS differential data input 31 NIND0 I Negative LVDS differential data input 32 GND P Ground 33 GND P Ground 34 RESET I GROUND F GROUN	20	GND	P	Ground
22 NINCLK 1 Negative LVDS differential CLK input 23 GND P Ground 24 PIND2 1 Positive LVDS differential data input 25 NIND2 1 Negative LVDS differential data input 26 GND P Ground 27 PIND1 I Positive LVDS differential data input 28 NIND1 I Negative LVDS differential data input 29 GND P Ground 30 PIND0 I Positive LVDS differential data input 31 NIND0 I Negative LVDS differential data input 32 GND P Ground 33 GND P Ground 34 RESET I Ground 34 RESET I GND, the chip is in teset state. This pin must neet the sequence of power on/off. Standby mode setting pin. Active low, Timing controller, output buffer, DAC and power circuit all off when STBYB is low 35 STBYB I Horizontal shift direction (source	21	PINCLK	I	Positive LVDS differential CLK input
23 GND	22	NINCLK	I	Negative LVDS differential CLK input
25 NIND2	23		P	•
25 NIND2	24	PIND2	I	Positive LVDS differential data input
26 GND P Ground 27 PIND1 I Positive LVDS differential data input 28 NIND1 I Negative LVDS differential data input 29 GND P Ground 30 PIND0 I Positive LVDS differential data input 31 NIND0 I Negative LVDS differential data input 32 GND P Ground 33 GND P Ground 34 RESET I GND, the chip is in reset state. This pin must neet the sequence of power on/off. 35 STBYB I Standby mode setting pin. Active low, Timing controller, output buffer, DAC and power circuit all off when STBYB is low This pin must meet the sequence of power on/off. 36 RL Horizontal shift direction (source output) selection RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT191→→S1) 37 VDD P Digital Power(+3.3V) Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top 39 GND P Ground 40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	25	NIND2	I	
PIND1				·
NIND1	27	PIND1	I	Positive LVDS differential data input
29 GND	28	NIND1	I	•
PIND0				·
NINDO				
32 GND P Ground 33 GND P Ground Global Reset pin Active low, If RESET connected to GND, the chip is in reset state. This pin must meet the sequence of power on/off. Standby mode setting pin. Active low, Timing controller, output buffer, DAC and power circuit all off when STBYB is low This pin must meet the sequence of power on/off. BL Horizontal shift direction (source output) selection RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT1919→→S1) Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top GND P Ground NC - No Connection TR = No Connection TO - No Connection GND P Ground GND P Ground GND P Ground GROD P Ground GROD P Ground GROD P Ground			Ţ	1.
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Global Reset pin. Active low, If RESET connected to GND, the chip'is in reset state. This pin must meet the sequence of power on/off. Standby mode setting pin. Active low, Timing controller, output buffer, DAC and power circuit all off when STBYB is low This pin must meet the sequence of power on/off. Horizontal shift direction (source output) selection RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT1919→→S1) VDD P Digital Power(+3.3V) Vertical shift direction(Gate output) selection TB = H, Forward,Top → Bottom TB = L, Reverse, Bottom → Top GRND P Ground NC No Connection No Connection No Connection No Connection GRND P Ground				
34 RESET I GND, the chip is in reset state. This pin must meet the sequence of power on/off. Standby mode setting pin. Active low, Timing controller, output buffer, DAC and power circuit all off when STBYB is low This pin must meet the sequence of power on/off. Horizontal shift direction (source output) selection RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT1919→→S1) VDD P Digital Power(+3.3V) Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top GND P Ground NC - No Connection NC - No Connection NC - No Connection GND P Ground			_	
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Standby mode setting pin. Active low, Timing controller, output buffer, DAC and power circuit all off when STBYB is low This pin must meet the sequence of power on/off. Horizontal shift direction (source output) selection RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT1919→→S1) VDD P Digital Power(+3.3V) Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top GND P Ground NC - No Connection NC - No Connection NO Connection TO Connection			_	
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STBYB				
Horizontal shift direction (source output) selection RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT1919→→S1) VDD P Digital Power(+3.3V) Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top GND P Ground NC No Connection NC No Connection VOD P Ground GND P Ground GND P Ground GROD P Ground	35	STBYB	I	
36 RL I RL=H, Forward (SOUT1→ SOUT2→→SOUT1920) RL=L, Reverse (SOUT1920→SOUT1919→→S1) 37 VDD P Digital Power(+3.3V) 37 VDD P Digital Power(+3.3V) 38 TB I TB = H, Forward, Top → Bottom TB = H, Forward, Top → Bottom Top 39 GND P Ground 40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground				This pin must meet the sequence of power on/off.
RL=L, Reverse (SOUT1920→SOUT1919→→S1) 37				Horizontal shift direction (source output) selection
37 VDD P Digital Power(+3.3V) Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom 38 TB I TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top Top 39 GND P Ground 40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	36	RL	1 >	RL=H, Forward (SOUT1→ SOUT2→→SOUT1920)
Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top GND P Ground NC - No Connection NC - No Connection Vertical shift direction(Gate output) selection TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top No Connection No Connection P No Connection GND P Ground VDD P Digital Power(+3.3V) GND P Ground				RL=L, Reverse (SOUT1920→SOUT1919→→S1)
38 TB I TB = H, Forward, Top → Bottom TB = L, Reverse, Bottom → Top 39 GND P Ground 40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	37	VDD	P	Digital Power(+3.3V)
TB = L, Reverse, Bottom → Top 39 GND P Ground 40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground				Vertical shift direction(Gate output) selection
39 GND P Ground 40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	38	ТВ	I	$TB = H$, Forward, Top \rightarrow Bottom
40 NC - No Connection 41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground				$TB = L$, Reverse, Bottom \rightarrow Top
41 NC - No Connection 42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	39	GND	P	Ground
42 NC - No Connection 43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	40	NC	-	No Connection
43 GND P Ground 44 VDD P Digital Power(+3.3V) 45 GND P Ground	41	NC	-	No Connection
44 VDD P Digital Power(+3.3V) 45 GND P Ground	42	NC	-	No Connection
45 GND P Ground	43	GND	P	Ground
	44	VDD	P	Digital Power(+3.3V)
46 NC - No Connection	45	GND	P	Ground
	46	NC	-	No Connection

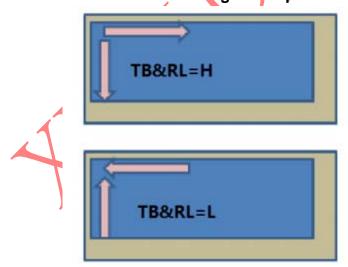


47	NC	-	No Connection
48	NC	-	No Connection
49	BISTEN	-	Enable built-in self test (BIST) function BISTEN=H, BIST mode BISTEN=L, Normal mode (Please leave it to GND when normal operation)
50	NC	-	No Connection
51	NC	-	No Connection
52	NC	-	No Connection
53	GND	P	Ground
54	VDD	P	Digital Power(+3.3V)
55	SELB	I	8/6 bit mode selection SELB=H, 8bit SELB=L, 6bit
56	NC	-	No Connection
57	VDD	P	Digital Power(+3.3V)
58	NC	-	No Connection
59	GND	P	Ground
60	NC	-	No Connection

Remark:

1. For "I/O", "I" is input; "O" is output, "P" is power; "C" is passive

Scan direction setting as the picture below;



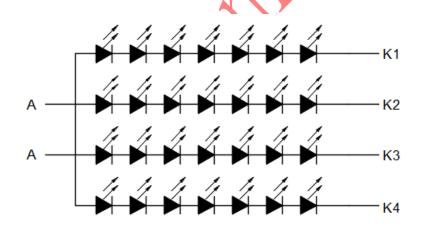


4.2 CN2

LED Board Pin Assignment:

CN2: FH28-10S-0.5SH (HRS)

NO	Symbol	Level	Description
1	PLED	P	LED anode power supply
2	PLED	P	LED anode power supply
3	NC	-	Keep floating
4	NTC1	О	LED Foil NTC
5	NIC2	О	LED FoiLNTC
6	NC	-	Keep floating
7	NLED1	P	LED cathode power supply
8	NLED2	P	LED cathode power supply
9	NLED3	P	LED cathode power supply
10	NLED4	P	LED cathode power supply





NTC1 — NTC2
NTC(NCP15XH103F0SRC)
LED 电路图



5. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-30 to 85	$^{\circ}$ C
Storage temperature	Tst	-40 to 90	$^{\circ}$
Power supply	VDD	-0.3V ~ 4.0	V

6.Electrical Characteristics

6.1 Description Dieplay Electronics

Ta=25℃

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Pov	ver supply	VDD	-	3.0	3.3	3.6	V
Power Sup	ply Input Current	$\mathbf{I}_{ ext{DD}}$	-	(-)	200	400	mA
Logic input	H level	V_{IHI}		0.7*VDD	-	VDD	V
signal Voltage	L level	V _{IL1}		GND	-	0.3*VDD	V

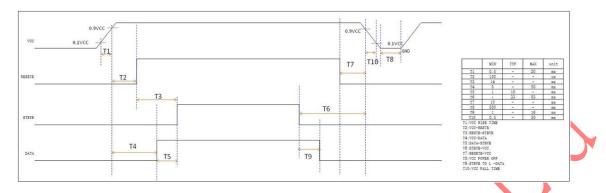
Notes:

1: Current Max is based "Gray 255"; Current Typ is based "Vertical Color Bar";





6.2 Power on/off Timing Sequence



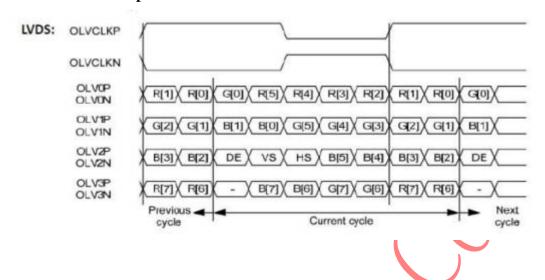
6.3.LVDS Signal Timing

Parameter	Symbol	Min	Тур	Max	Unit
Clock frequency	Rx FCLK	40.00	40.06	41.60	MHz
Horizontal Display Area	Thd		1280		DCLK
1horizontal line	Th	1342	1346	1398	
Vertical Display Area	Tvd		480		DCLK
1 vertical field	Tv	498	496	504	
Frame rate	FR		60		HZ



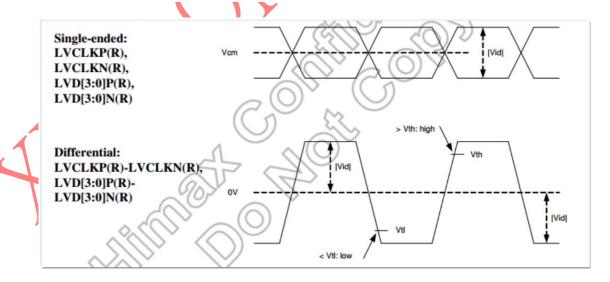


6.4. LVDS input 8 bit LVDS input



6.5.LVDS Characteristics

1001-10011 -1005-1001				<u> </u>		
Parameter	Symbol Condition		Unit			
Farameter	Symbol	Condition	Min.	Typ.	Max.	Offic
Differential input high Threshold voltage	Vth	Vcm=1.2V	+0.10		<u></u>	٧
Differential input low threshold voltage	VtI	Vcm=1.2V	-	5,6	-0:10	٧
Differential input common Mode voltage	Vсм	-	1	1.2	1.7- Vid /2	٧
LVDS input voltage	VINLV		0.7		£ % 1.7	٧
Differential input voltage	Vid		0.1	(1)88 3°	0.6	٧
Differential input leakage Current	Ilvleak	-	-10	2021-05	+10	μА

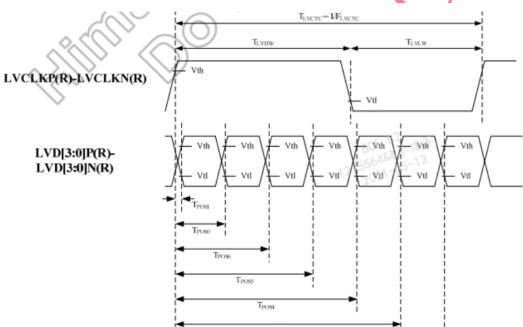




6.6.LVDS AC Characteristics

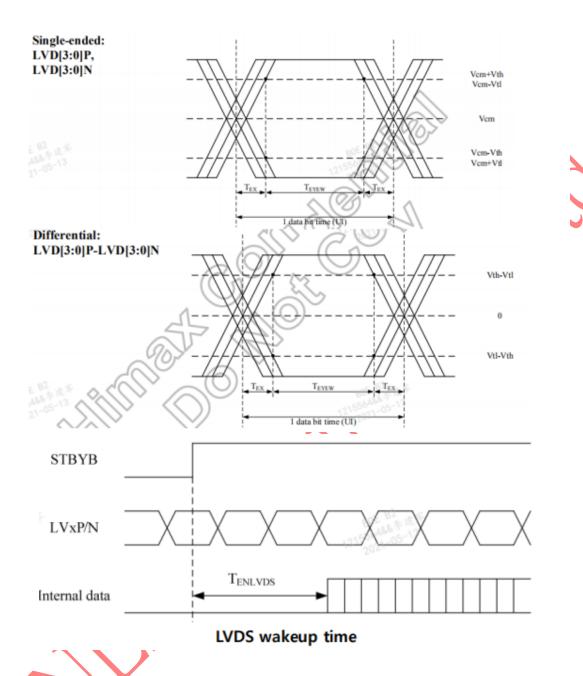
(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, Top=-40~105°C)

Danamatan	Combal		Spec.	1.1-14	
Parameter	Symbol	Min.	Тур.	Max.	Unit
Clock frequency (1-port/2-port)	FLVCYC	15	2//	105/95	MHz
Clock period (1-port/2-port)	TLVCYC	9.52/9.09	(3) - (-	ns
1 data bit time	UI	3///	1/7	() -	TLVCYC
Clock high time	TLVCH	0. (1)	4	9/ -	UI
Clock low time	T _L VCL (500	3)) -	UI
Position 1	TPOS1	-0.2	0	0.2	UI
Position 0	Tposo C	0.8		1.2	UI
Position 6	Tpos6	1.8	(2	2.2	UI
Position 5	TPOS5	2.8	3	3.2	UI
Position 4	TPOS4	3.8	4	4.2	UI
Position 3	TPOS3	4.8	5	5.2	UI
Position 2	TPOS2	5.8	6	6.2	UI
Input eye width	TEYEW	0.6	ENE BE	# A-	UI
Input eye border	T _{EX} (7) -	8844	0.2	UI
LVDS wake up time	TENLVOS	9 -	1215201-0	150	us
LVDS clock to clock skew	T _{skew_EO}	-1/7	702	1/7	UI









Note: AC and DS characteristics of the above LVDS is an acceptablespeci

fication for the driver IC, and the system output specification needs to be te sted and validated withthe entire module to meet the IC requirements.



7. Backlight Characteristics

Item	syb	Min	Тур	Max	Unit	Condition
Voltage	Vf	18.9	22.4	23.8	V	Note1
Number of LED	-	28			pcs	-
Life	-	-	30000	-	hrs	Note2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25°C and If 40mA*4=160mA.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25% and IL=160 mA. The LED lifetime could be decreased if operating IL is larger than 160mA.



8. Electro-Optical Characteristics

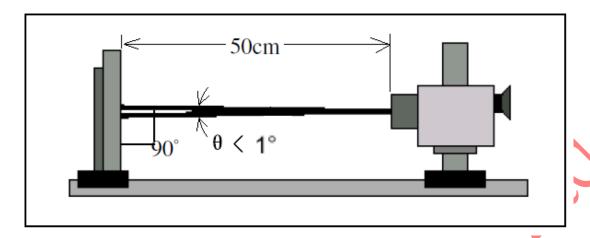
Item		Symbol	Condition	Min	Тур	Max	Unit	Note
Response time			25℃	-	-	25	ms	4
		Tr+Tf	-20℃	_	-	200		
			-30°C	-	-	380		
Uniformity		δ		75	80		%	
(Five point)		WHITE		/3	80	- 4		
Contrast ratio		Cr		900	1000	-	-	3 ,5
Surface Luminance		Lv		700	800		(<u>-</u>)	3 ,7
	Horizontal	X+	CR > 10	80	85		deg	6
Viewing angle range		Х-		80	85		deg	
	Vertical	y+		80	85	-	deg	
ungie runge		у-		80	85	-	deg	
	White	X	$\theta = \Phi = 0^{\circ}$	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	Red	X	$\theta = \Phi = 0_{\circ}$	TBD	TBD	TBD		
Color filter chromaticity (x, y)		Y		TBD	TBD	TBD		7
	Green	X		TBD	TBD	TBD	-	/
		Y	Ψ-0	TBD	TBD	TBD		
	Blue	X	$\theta = \Phi = 0^{\circ}$	TBD	TBD	TBD		
		у	$\nabla - \Psi = 0$	TBD	TBD	TBD		

Note 1: Ambient temperature=25°C±2°C

Note 2: To be measured in the dark room with backlight unit.

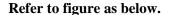
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).

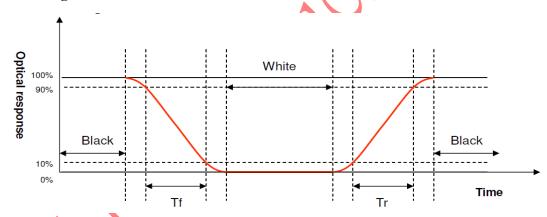




Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.





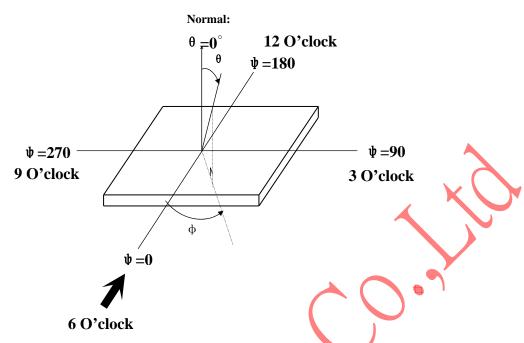
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

Note 6. Definition of viewing angle

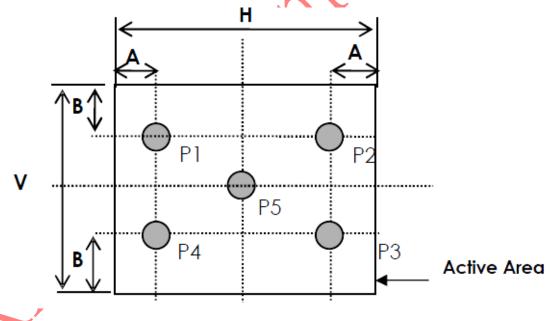
Viewing angle is the angle at which the contrast ratio is greater than 10 for TFT module. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.





Note 7. Surface luminance is the LCD surface from the surface with all pixels displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity



A:5 mm B:5 mm H,V: Active Area

Light spot size Æ=7mm, 500mm distance from the LCD surface to detector lens measurement instrument is TOPCON's luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%

Lv = Average Surface Luminance with all white pixels (P5)



9. Reliability Test

This standard reliability test is done only for the first lot of MP products. Customer and supplier must hold a discussion if other reliability test is requested by customer.

NO.	Test Item	Test Condition	Remarks		
1	High temperature storage	90°C,500 H	Note1 IEC60068-2-1:2007,GB2423.2-2008		
2	Low temperature storage	-40℃, 500 H	IEC60068-2-1:2007 GB2423.1-2008		
3	High temperature operation	85℃, 500 H	IEC60068-2-1:2007 GB2423.2-2008		
4	Low temperature operation	-30°C, 500 H	IEC60068-2-1:2007 GB2423.1-2008		
5	High temperature /humidity storage	60°C,90% RH,500H	Note2 IEC60068-2-78 :2001 GB/T2423.3—2006		
6	Temperature Cycle (Non operation)	-40°C/85°C, 200 cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002		
7	Electrostatic Discharge	- - -	R=330 Ω ,C=150pF Contact = \pm 8 kV, class B; Air = \pm 15 kV, class B; 1 time for each point.		

10. Precautions for Operation and Storage

1. Precautions for Operation

- (1)Since LCD panel made of glass,in order to prevent from glass broken or color tone change,please do not apply any mechanical shock or impact or excessive force to it when installing the LCD module.
- (2)If LCD panel is broken and liquid crystal substance leaks out and contact your skin or clothes, please immediately wash it off by using soap and water.
- (3)The polarizer on the LCD surface is soft and easily scratched. Please be careful when handling.
- (4)If LCD surface becomes contaminated, please wipe it off gently by using mois ten soft cloth with normal hexane, do not use acetone, ketone, ethanol, alcohol or water. If there is saliva or water on the LCD surface, please wipe it off immediate ly.
- (5) When handing LCD module, please be sure that the body and the tools are properly grounded. And do not touch I/F pins with bare hands or contaminate I/F pins.
- (6)Do not attempt to disassemble or process the LCD module.
- (7)LCD module should be used under recommended operating conditions shown in chapter 6 and 7.
- (8)Response time will be extremely slower at lower temperature than at specified temperature and LCD will show different color when at higher temperature. The phenomenon will disappear when returning to specified condition.
- (9)Foggy dew,moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage,the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

1. Precautions for Storage

- 1)Please store LCD module in a dark place, avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
- (2)Keep the environment temperature at between 10° C and 35° C and at normal humidity. Avoid high temperature, high humidity or temperature below 0° C.
- (3)That keeps the LCD modules stored in the container shipped from supplier be fore using them is recommended.



(4)Do not leave any article on the LCD module surface for an extended period of time.

2. Warranty period

Warrants for a period of 12 Months from the shipping date when stored or used under normal condition.





11. Package Specification

TBD

